In-Man Kang

List of Publications by Year in Descending Order

138 papers	1,042 citations	16 h-index	27 g-index
164 ext. papers	1,337 ext. citations	2.2 avg, IF	4.4 L-index

#	Paper	IF	Citations
138	Flexible Sol-Gel-Processed YO RRAM Devices Obtained via UV/Ozone-Assisted Photochemical Annealing Process.. *Materials*, **2022**, 15,	3.5	1
137	Room-Temperature High-Detectivity Flexible Near-Infrared Photodetectors with Chalcogenide Silver Telluride Nanoparticles.. *ACS Omega*, **2022**, 7, 10262-10267	3.9	0
136	Design of Capacitorless DRAM Based on Polycrystalline Silicon Nanotube Structure. *IEEE Access*, **2021**, 9, 163675-163685	3.5	0
135	Improving of Sensitivity of PbS Quantum Dot Based SWIR Photodetector Using P3HT. *Materials*, **2021**, 14,	3.5	1
134	Experimental and simulation study of power performance improvement of GaN PIN betavoltaic cell. *International Journal of Energy Research*, **2021**, 45, 17622-17630	4.5	1
133	Effects of Proton Irradiation on the Current Characteristics of SiN-Passivated AlGaN/GaN MIS-HEMTs Using a TMAH-Based Surface Pre-Treatment. *Micromachines*, **2021**, 12,	3.3	2
132	Numerical Design of Carrier Transporting Layer in Top-Gate InGaZnO Thin-Film Transistors for Controlling Potential Energy. *Journal of Nanoscience and Nanotechnology*, **2021**, 21, 3847-3852	1.3	0
131	Improved Negative Bias Stress Stability of Sol-Gel-Processed Li-Doped SnO2 Thin-Film Transistors. *Electronics (Switzerland)*, **2021**, 10, 1629	2.6	1
130	Design optimization of GaN diode with p-GaN multi-well structure for high-efficiency betavoltaic cell. *Nuclear Engineering and Technology*, **2021**, 53, 1284-1288	2.6	2
129	Polycrystalline-Silicon-MOSFET-Based Capacitorless DRAM With Grain Boundaries and Its Performances. *IEEE Access*, **2021**, 1-1	3.5	1
128	Influence of Active Channel Layer Thickness on SnO2 Thin-Film Transistor Performance. *Electronics (Switzerland)*, **2021**, 10, 200	2.6	3
127	Single-event transient characteristics of vertical gate-all-around junctionless field-effect transistor on bulk substrate. *Applied Physics A: Materials Science and Processing*, **2021**, 127, 1	2.6	3
126	Design of a Capacitorless Dynamic Random Access Memory Based on Ultra-Thin Polycrystalline Silicon Junctionless Field-Effect Transistor with Dual-Gate. *Journal of Nanoscience and Nanotechnology*, **2021**, 21, 4223-4229	1.3	0
125	Analysis of Grain Boundary Dependent Memory Characteristics in Poly-Si One-Transistor Dynamic Random-Access Memory. *Journal of Nanoscience and Nanotechnology*, **2021**, 21, 4216-4222	1.3	0
124	The Effect of Grain Boundary on Electrical Characteristics in the Source and Drain Regions of Polycrystalline Silicon Based in One Transistor Dynamic Random Access Memory. *Journal of Nanoscience and Nanotechnology*, **2021**, 21, 4258-4267	1.3	
123	Design and Analysis of DC/DC Boost Converter Using Vertical GaN Power Device. *Journal of Nanoscience and Nanotechnology*, **2021**, 21, 4320-4324	1.3	
122	Design of a Capacitorless Dynamic Random Access Memory Based on Junctionless Dual-Gate Field-Effect Transistor with a Silicon-Germanium/Silicon Nanotube. *Journal of Nanoscience and Nanotechnology*, **2021**, 21, 4235-4242	1.3	0

121	Extremely bias stress stable enhancement mode sol-gel-processed SnO2 thin-film transistors with Y2O3 passivation layers. *Applied Surface Science*, **2021**, 559, 149971	6.7	7
120	Design and optimization of GaN -based betavoltaic cell for enhanced output power density. *International Journal of Energy Research*, **2021**, 45, 799-806	4.5	2
119	Fluoropolymer-based organic memristor with multifunctionality for flexible neural network system. *Npj Flexible Electronics*, **2021**, 5,	10.7	6
118	Effect of High-Speed Blade Coating on Electrical Characteristics in Polymer Based Transistors. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 5486-5490	1.3	2
117	Effect of Mg Doping on the Electrical Performance of a Sol-Gel-Processed SnO2 Thin-Film Transistor. *Electronics (Switzerland)*, **2020**, 9, 523	2.6	9
116	Fabrication of AlGaN/GaN MISHEMT with dual-metal gate electrode and its performances. *Applied Physics A: Materials Science and Processing*, **2020**, 126, 1	2.6	6
115	Effects of Contact Potential and Sidewall Surface Plane on the Performance of GaN Vertical Nanowire MOSFETs for Low-Voltage Operation. *IEEE Transactions on Electron Devices*, **2020**, 67, 1547-1552	2.9	4
114	Enhancement Mode Flexible SnO2 Thin Film Transistors Via a UV/Ozone-Assisted Sol-Gel Approach. *IEEE Access*, **2020**, 8, 123013-123018	3.5	5
113	Recessed-Gate GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistor Using a Dual Gate-Insulator Employing TiO2/SiN. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4678-4683	1.3	1
112	Analysis of Logic Inverter Based on Polycrystalline Silicon with Single Grain Boundary. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6616-6621	1.3	
111	Analysis of the Sensing Margin of Silicon and Poly-Si 1T-DRAM. *Micromachines*, **2020**, 11,	3.3	5
110	Sol-Gel Processed Yttrium-Doped SnO2 Thin Film Transistors. *Electronics (Switzerland)*, **2020**, 9, 254	2.6	12
109	Numerical Analysis on Effective Mass and Traps Density Dependence of Electrical Characteristics of a-IGZO Thin-Film Transistors. *Electronics (Switzerland)*, **2020**, 9, 119	2.6	7
108	Application of Genetic Algorithm for More Efficient Multi-Layer Thickness Optimization in Solar Cells. *Energies*, **2020**, 13, 1726	3.1	5
107	Analysis of CMOS Logic Inverter Based on Gate-All-Around Field-Effect Transistors with the Strained-Silicon Layer for Improving the Switching Performances. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6632-6637	1.3	
106	Design and Analysis of Metal-Oxide-Semiconductor Field-Effect Transistor-Based Capacitorless One-Transistor Embedded Dynamic Random-Access Memory with Double-Polysilicon Layer Using Grain Boundary for Hole Storage. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 6596-6602	1.3	
105	Charge Based Current-Voltage Model for the Silicon on Insulator Junctionless Field-Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4920-4925	1.3	
104	Theoretical Analysis of Prospects of Organic Photovoltaics as a Multi-Functional Solar Cell and Laser Power Converter for Wireless Power Transfer. *Journal of Nanoscience and Nanotechnology*, **2020**, 20, 4878-4883	1.3	

103	Improved negative bias stability of sol-gel processed Ti-doped SnO2 thin-film transistors. *Semiconductor Science and Technology*, **2020**, 35, 115023	1.8	5
102	Contact line curvature-induced molecular misorientation of a surface energy patterned organic semiconductor in meniscus-guided coating. *Applied Surface Science*, **2020**, 504, 144362	6.7	7
101	Polycrystalline silicon metal-oxide-semiconductor field-effect transistor-based stacked multi-layer one-transistor dynamic random-access memory with double-gate structure for the embedded systems. *Japanese Journal of Applied Physics*, **2020**, 59, SGGB01	1.4	3
100	Control of silver nanowire-elastomer nanocomposite networks through elaborate direct printing for ultrathin and stretchable strain sensors. *Composites Science and Technology*, **2020**, 200, 108471	8.6	5
99	Simulation of capacitorless dynamic random access memory based on junctionless FinFETs using grain boundary of polycrystalline silicon. *Applied Physics A: Materials Science and Processing*, **2020**, 126, 1	2.6	2
98	Fabrication of AlGaN/GaN Fin-Type HEMT Using a Novel T-Gate Process for Improved Radio-Frequency Performance. *IEEE Access*, **2020**, 8, 139156-139160	3.5	4
97	Gallium Nitride Normally Off MOSFET Using Dual-Metal-Gate Structure for the Improvement in Current Drivability. *Electronics (Switzerland)*, **2020**, 9, 1402	2.6	2
96	Design and Analysis of Gallium Nitride-Based p-i-n Diode Structure for Betavoltaic Cell with Enhanced Output Power Density. *Micromachines*, **2020**, 11,	3.3	2
95	One-Transistor Dynamic Random-Access Memory Based on Gate-All-Around Junction-Less Field-Effect Transistor with a Si/SiGe Heterostructure. *Electronics (Switzerland)*, **2020**, 9, 2134	2.6	2
94	The Crucial Role of Quaternary Mixtures of Active Layer in Organic Indoor Solar Cells. *Energies*, **2019**, 12, 1838	3.1	10
93	A polycrystalline-silicon dual-gate MOSFET-based 1T-DRAM using grain boundary-induced variable resistance. *Applied Physics Letters*, **2019**, 114, 183503	3.4	10
92	Analysis of Electrical Characteristics of InAlGaN/GaN-Based High Electron Mobility Transistors with AlGaN Back Barriers. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6008-6015	1.3	1
91	Capacitorless One-Transistor Dynamic Random-Access Memory Based on Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor with Si/SiGe Heterojunction and Underlap Structure for Improvement of Sensing Margin and Retention Time. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6023-6030	1.3	3
90	Design Optimization and Analysis of InGaAs/InAs/InGaAs Heterojunction-Based Electron Hole Bilayer Tunneling FETs. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6070-6076	1.3	2
89	Design Optimization of InGaAs/GaAsSb-Based -Type Gate-All-Around Arch-Shaped Tunneling Field-Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6762-6766	1.3	0
88	Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect. *IEEE Electron Device Letters*, **2019**, 40, 566-569	4.4	15
87	Deep Sub-60 mV/decade Subthreshold Swing in AlGaN/GaN FinMISHFETs with M-Plane Sidewall Channel. *IEEE Transactions on Electron Devices*, **2019**, 66, 1699-1703	2.9	8
86	Design and analysis of logic inverter using antimonide-based compound semiconductor junctionless transistor. *Applied Physics A: Materials Science and Processing*, **2019**, 125, 1	2.6	1

85	Analysis of operation characteristics of junctionless poly-Si 1T-DRAM in accumulation mode. *Semiconductor Science and Technology*, **2019**, 34, 105007	1.8	4
84	Importance of Blade-Coating Temperature for Diketopyrrolopyrrole-based Thin-Film Transistors. *Crystals*, **2019**, 9, 346	2.3	4
83	Simulation for Electrical Performances of the Capacitorless Dynamic Random Access Memory Based on Junctionless FinFETs. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6755-6761	1.3	
82	Effect of Annealing Ambient on SnO2 Thin Film Transistors Fabricated via An Ethanol-based Sol-gel Route. *Electronics (Switzerland)*, **2019**, 8, 955	2.6	9
81	Design and Optimization of Germanium-Based Gate-Metal-Core Vertical Nanowire Tunnel FET. *Micromachines*, **2019**, 10,	3.3	5
80	Microwave analysis of SiGe heterojunction double-gate tunneling field-effect transistor through its small-signal equivalent circuit. *International Journal of RF and Microwave Computer-Aided Engineering*, **2019**, 29, e21678	1.5	2
79	Capacitorless one-transistor dynamic random-access memory based on asymmetric double-gate Ge/GaAs-heterojunction tunneling field-effect transistor with n-doped boosting layer and drain-underlap structure. *Japanese Journal of Applied Physics*, **2018**, 57, 04FG03	1.4	7
78	Performance comparison between p□□ and p□ junction tunneling field-effect transistors. *Japanese Journal of Applied Physics*, **2018**, 57, 06HC01	1.4	2
77	Low voltage operation of GaN vertical nanowire MOSFET. *Solid-State Electronics*, **2018**, 145, 1-7	1.7	19
76	A Novel Analysis of ${L}_{text{gd}}$ Dependent-1/ ${f}$ Noise in In0.08Al0.92N/GaN. *IEEE Electron Device Letters*, **2018**, 39, 1552-1555	4.4	3
75	Design Optimization of Ge/GaAs-Based Heterojunction Gate-All-Around (GAA) Arch-Shaped Tunneling Field-Effect Transistor (A-TFET). *Journal of Nanoscience and Nanotechnology*, **2018**, 18, 6602-6605	1.3	
74	Normally-off AlGaN/GaN-based MOS-HEMT with self-terminating TMAH wet recess etching. *Solid-State Electronics*, **2018**, 141, 7-12	1.7	6
73	Simulation of One-Transistor Dynamic Random-Access Memory Based on Symmetric Double-Gate Si Junctionless Transistor. *Journal of Nanoscience and Nanotechnology*, **2018**, 18, 6593-6597	1.3	
72	Analysis of tunneling field-effect transistor with germanium source junction using small-signal equivalent circuit. *Microwave and Optical Technology Letters*, **2018**, 60, 2922-2927	1.2	1
71	1/f-Noise in AlGaN/GaN Nanowire Omega-FinFETs. *IEEE Electron Device Letters*, **2017**, 38, 252-254	4.4	17
70	Electrical Performances of InN/GaN Tunneling Field-Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 8355-8359	1.3	1
69	Performance enhancement of AlGaN/GaN nanochannel omega-FinFET. *Solid-State Electronics*, **2017**, 129, 196-199	1.7	4
68	Design Optimization and Analysis of InGaAs-Based Gate-All-Around (GAA) Junctionless Field-Effect Transistor (JLFET). *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 8350-8354	1.3	

67	Effect of Electric Fringe-Field on Low-Power and Radio-Frequency Performances of Sub-10 nm Junctionless Transistors with Hetero-Dielectric Spacer Structure. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7140-7144	1.3	
66	Fully Coupled Finite-Element Analysis for Surface Discharge on Solid Insulation in Dielectric Liquid With Experimental Validation. *IEEE Transactions on Magnetics*, **2016**, 52, 1-4	2	7
65	Design Optimization of AlN/GaN-Based Double-Heterojunction Fin-Type High Electron Mobility Transistors for High On-State Current. *Journal of Nanoscience and Nanotechnology*, **2016**, 16, 10193-10198	1.3	2
64	. *IEEE Electron Device Letters*, **2016**, 37, 855-858	4.4	25
63	Design optimization of Si/Ge-based heterojunction arch-shaped gate-all-around (GAA) tunneling field-effect transistor (TFET) which applicable for future mobile communication systems **2016**,		1
62	DC and RF Analysis of Geometrical Parameter Changes in the Current Aperture Vertical Electron Transistor. *Journal of Electrical Engineering and Technology*, **2016**, 11, 1763-1768	1.4	
61	TMAH-based wet surface pre-treatment for reduction of leakage current in AlGaN/GaN MIS-HEMTs. *Solid-State Electronics*, **2016**, 124, 54-57	1.7	12
60	Design optimization of vertical nanowire tunneling field-effect transistor based on AlGaSb/InGaAs heterojunction layer. *Current Applied Physics*, **2016**, 16, 681-685	2.6	4
59	Effects of sidewall MOS channel on performance of AlGaN/GaN FinFET. *Microelectronic Engineering*, **2015**, 147, 155-158	2.5	17
58	AlGaN/GaN FinFET With Extremely Broad Transconductance by Side-Wall Wet Etch. *IEEE Electron Device Letters*, **2015**, 36, 1008-1010	4.4	45
57	Characteristics of temperature rise in variable inductor employing magnetorheological fluid driven by a high-frequency pulsed voltage source. *Journal of Applied Physics*, **2015**, 117, 17D508	2.5	1
56	Short-Channel Tunneling Field-Effect Transistor with Drain-Overlap and Dual-Metal Gate Structure for Low-Power and High-Speed Operations. *Journal of Nanoscience and Nanotechnology*, **2015**, 15, 7430-5	1.3	5
55	Control of transconductance in high performance AlGaN/GaN FinFETs **2015**,		4
54	First demonstration of GaN-based vertical nanowire FET with top-down approach **2015**,		9
53	Design and analysis of Si-based arch-shaped gate-all-around (GAA) tunneling field-effect transistor (TFET). *Current Applied Physics*, **2015**, 15, 208-212	2.6	19
52	Design and Analysis of CMOS-Compatible III-V Compound Electron-Hole Bilayer Tunneling Field-Effect Transistor for Ultra-Low-Power Applications. *Journal of Nanoscience and Nanotechnology*, **2015**, 15, 7486-92	1.3	2
51	Suppression of current collapse in AlGaN/GaN MISHFET with carbon- doped GaN/undoped GaN multi-layered buffer structure. *Physica Status Solidi (A) Applications and Materials Science*, **2015**, 212, 1116-1121	1.6	24
50	Analyses on RF Performances of Silicon-Compatible InGaAs-Based Planar-Type and Fin-Type Junctionless Field-Effect Transistors. *Journal of Nanoscience and Nanotechnology*, **2015**, 15, 7615-9	1.3	2

49	Fabrication of high performance AlGaN/GaN FinFET by utilizing anisotropic wet etching in TMAH solution **2015**,		3
48	Electrical Characteristics of Enhancement-Mode n-Channel Vertical GaN MOSFETs and the Effects of Sidewall Slope. *Journal of Electrical Engineering and Technology*, **2015**, 10, 1131-1137	1.4	4
47	Electrohydrodynamic Analysis of Dielectric Guide Flow Due to Surface Charge Density Effects in Breakdown Region. *Journal of Electrical Engineering and Technology*, **2015**, 10, 647-652	1.4	1
46	GaN junctionless trigate field-effect transistor with deep-submicron gate length: Characterization and modeling in RF regime. *Japanese Journal of Applied Physics*, **2014**, 53, 118001	1.4	7
45	Dependence of device performances on fin dimensions in AlGaN/GaN recessed-gate nanoscale FinFET **2014**,		1
44	Highly enhanced charge injection and bulk transport in organic gap-type diodes via one-pot treatment process: experiment and simulation. *Micro and Nano Letters*, **2014**, 9, 887-890	0.9	
43	Heteromaterial gate tunneling field-effect transistor for high-speed and radio-frequency applications. *Journal of Nanoscience and Nanotechnology*, **2014**, 14, 8136-40	1.3	3
42	Design of a recessed-gate GaN-based MOSFET using a dual gate dielectric for high-power applications. *Journal of the Korean Physical Society*, **2014**, 65, 1579-1584	0.6	2
41	Improvement of Current Efficiency at High Field Regime Via Description of Roll-off Characteristic in Model Device of OLEDs. *Molecular Crystals and Liquid Crystals*, **2014**, 599, 79-85	0.5	2
40	Fabrication and Characterization of GaN-based Light-emitting Diode (LED) with Triangle-type Structure. *Molecular Crystals and Liquid Crystals*, **2014**, 599, 163-169	0.5	1
39	Investigation of InAs/InGaAs/InP Heterojunction Tunneling Field-Effect Transistors. *Journal of Electrical Engineering and Technology*, **2014**, 9, 1654-1659	1.4	3
38	Evaluation of Radio-Frequency Performance of Gate-All-Around Ge/GaAs Heterojunction Tunneling Field-Effect Transistor with Hetero-Gate-Dielectric by Mixed-Mode Simulation. *Journal of Electrical Engineering and Technology*, **2014**, 9, 2070-2078	1.4	1
37	More Accurate and Reliable Extraction of Tunneling Resistance in Tunneling FET and Verification in Small-Signal Circuit Operation. *IEEE Transactions on Electron Devices*, **2013**, 60, 3318-3324	2.9	8
36	InGaAs/InP heterojunction-channel tunneling field-effect transistor for ultra-low operating and standby power application below supply voltage of 0.5 V. *Current Applied Physics*, **2013**, 13, 2051-2054	2.6	8
35	Highly sensitive ion sensor based on the MOSFET–BJT hybrid mode of a gated lateral BJT. *Sensors and Actuators B: Chemical*, **2013**, 181, 44-49	8.5	5
34	Simulation study on effect of drain underlap in gate-all-around tunneling field-effect transistors. *Current Applied Physics*, **2013**, 13, 1143-1149	2.6	32
33	Mixed-Mode Simulation of Nanowire Ge/GaAs Heterojunction Tunneling Field-Effect Transistor for Circuit Applications. *IEEE Journal of the Electron Devices Society*, **2013**, 1, 48-53	2.3	7
32	Compound Semiconductor Tunneling Field-Effect Transistor Based on Ge/GaAs Heterojunction with Tunneling-Boost Layer for High-Performance Operation. *Japanese Journal of Applied Physics*, **2013**, 52, 04CC04	1.4	3

31	Simulation for silicon-compatible InGaAs-based junctionless field-effect transistor using InP buffer layer. *Semiconductor Science and Technology*, **2013**, 28, 105007	1.8	3
30	Analysis on RF parameters of nanoscale tunneling field-effect transistor based on InAs/InGaAs/InP heterojunctions. *Journal of Nanoscience and Nanotechnology*, **2013**, 13, 8133-6	1.3	1
29	Silicon-compatible high-hole-mobility transistor with an undoped germanium channel for low-power application. *Applied Physics Letters*, **2013**, 103, 222102	3.4	6
28	Rigorous Design and Analysis of Tunneling Field-Effect Transistor with Hetero-Gate-Dielectric and Tunneling-Boost n-Layer. *IEICE Transactions on Electronics*, **2013**, E96.C, 644-648	0.4	1
27	Design Optimization of Silicon-based Junctionless Fin-type Field-Effect Transistors for Low Standby Power Technology. *Journal of Electrical Engineering and Technology*, **2013**, 8, 1497-1502	1.4	2
26	Simulation study on scaling limit of silicon tunneling field-effect transistor under tunneling-predominance. *IEICE Electronics Express*, **2012**, 9, 828-833	0.5	2
25	Design optimization of vertical double-gate tunneling field-effect transistors. *Journal of the Korean Physical Society*, **2012**, 61, 1679-1682	0.6	3
24	Design optimization of tunneling field-effect transistor based on silicon nanowire PNPN structure and its radio frequency characteristics. *Current Applied Physics*, **2012**, 12, 673-677	2.6	18
23	Performance of Gate-All-Around Tunneling Field-Effect Transistors Based on Si1-x Gex Layer. *IEICE Transactions on Electronics*, **2012**, E95.C, 814-819	0.4	4
22	Fabrication and Characterization of a GaN Light-emitting Diode (LED) with a Centered Island Cathode. *Journal of the Optical Society of Korea*, **2012**, 16, 349-353		3
21	Extraction of T-Type Substrate Resistance Components for Radio-Frequency Metal□Oxide□Semiconductor Field-Effect Transistors Based on Two-Port□S-Parameter Measurement. *Japanese Journal of Applied Physics*, **2012**, 51, 111201	1.4	
20	Silicon-compatible compound semiconductor tunneling field-effect transistor for high performance and low standby power operation. *Applied Physics Letters*, **2011**, 99, 243505	3.4	30
19	. *IEEE Transactions on Electron Devices*, **2011**, 58, 1388-1396	2.9	124
18	. *IEEE Transactions on Electron Devices*, **2011**, 58, 4164-4171	2.9	65
17	Compact modeling of silicon nanowire MOSFET for radio frequency applications. *Microwave and Optical Technology Letters*, **2011**, 53, 471-473	1.2	1
16	Radio Frequency Performance of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. *Japanese Journal of Applied Physics*, **2011**, 50, 124301	1.4	9
15	Non-Quasi-Static Modeling of Silicon Nanowire Metal□Oxide□Semiconductor Field-Effect Transistor and Its Model Verification up to 1 THz. *Japanese Journal of Applied Physics*, **2010**, 49, 110206	1.4	5
14	Investigation of source-to-drain capacitance by DIBL effect of silicon nanowire MOSFETs. *IEICE Electronics Express*, **2010**, 7, 1499-1503	0.5	3

13	RF Model of BEOL Vertical Natural Capacitor (VNCAP) Fabricated by 45-nm RF CMOS Technology and Its Verification. *IEEE Electron Device Letters*, **2009**, 30, 538-540	4.4	7
12	Five-Step (PadPad ShortPad OpenShortOpen) De-Embedding Method and Its Verification. *IEEE Electron Device Letters*, **2009**, 30, 398-400	4.4	24
11	. *IEEE Electron Device Letters*, **2009**, 30, 404-406	4.4	11
10	Extraction of pi-Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *IEEE Electron Device Letters*, **2007**, 28, 425-427	4.4	7
9	A New Noise Parameter Model of Short-Channel MOSFETs. *Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE*, **2007**,		8
8	Separate Extraction of Gate Resistance Components in RF MOSFETs. *IEEE Transactions on Electron Devices*, **2007**, 54, 1459-1463	2.9	21
7	2.4 GHz ISM-Band Receiver Design in a 0.18 $mu{hbox{m}}$ Mixed Signal CMOS Process. *IEEE Microwave and Wireless Components Letters*, **2007**, 17, 736-738	2.6	5
6	Active and Passive RF Device Compact Modeling in CMOS Technoloies **2006**,		2
5	Non-quasi-static small-signal modeling and analytical parameter extraction of SOI FinFETs. *IEEE Nanotechnology Magazine*, **2006**, 5, 205-210	2.6	63
4	Extraction and modeling of gate electrode resistance in rf MOSFETs **2005**,		1
3	The analysis of dark signals in the CMOS APS imagers from the characterization of test structures. *IEEE Transactions on Electron Devices*, **2004**, 51, 178-184	2.9	84
2	Effects of electrical stress on mid-gap interface trap density and capture cross sections in n-MOSFETs characterized by pulsed interface probing measurements. *Microelectronics Reliability*, **2004**, 44, 47-51	1.2	
1	Enhanced switching ratio of solGel-processed Y2O3 RRAM device by suppressing oxygen-vacancy formation at high annealing temperature. *Semiconductor Science and Technology*,	1.8	2