Ni Tianming

List of Publications by Year
in descending order

40 papers	657 citations	687363 13 h-index	580821 25 g-index
41 all docs	41 docs citations	41 times ranked	396 citing authors

#	Article	IF	Citations
1	Novel Quadruple-Node-Upset-Tolerant Latch Designs With Optimized Overhead for Reliable Computing in Harsh Radiation Environments. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 404-413.	4.6	49
2	Design of True Random Number Generator Based on Multi-Stage Feedback Ring Oscillator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1752-1756.	3.0	17
3	Anti-interference low-power double-edge triggered flip-flop based on C-elements. Tsinghua Science and Technology, 2022, 27, 1-12.	6.1	8
4	Fortune: A New Fault-Tolerance TSV Configuration in Router-Based Redundancy Structure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3182-3187.	2.7	0
5	Calibration of SQUID Magnetometers in Multichannel MCG System Based on Bi-Planar Coil. IEEE Transactions on Instrumentation and Measurement, 2022, 71, 1-9.	4.7	9
6	Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications. IEEE Transactions on Device and Materials Reliability, 2022, 22, 282-295.	2.0	34
7	SCLCRL: Shuttling C-elements based Low-Cost and Robust Latch Design Protected against Triple Node Upsets in Harsh Radiation Environments. , 2022, , .		3
8	Broadcast-TDMA: A Cost-Effective Fault-Tolerance Method for TSV Lifetime Reliability Enhancement. IEEE Design and Test, 2022, 39, 34-42.	1.2	3
9	A Novel TDMA-Based Fault Tolerance Technique for the TSVs in 3D-ICs Using Honeycomb Topology. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 724-734.	4.6	39
10	Cross-Layer Dual Modular Redundancy Hardened Scheme of Flip-Flop Design Based on Sense-Amplifier. Journal of Circuits, Systems and Computers, 2021, 30, 2120003.	1.5	1
11	A Cost-Effective TSV Repair Architecture for Clustered Faults in 3-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1952-1956.	2.7	29
12	A Nanofluidic Sensor for Real-Time Detection of Ultratrace Contaminant Particles in IC Fabrication. IEEE Sensors Journal, 2021, 21, 755-764.	4.7	4
13	Chip test pattern reordering method using adaptive test to reduce cost for testing of ICs. IEICE Electronics Express, 2021, 18, 20200420-20200420.	0.8	7
14	A Test Method for Large-size TSV Considering Resistive Open Fault and Leakage Fault Coexistence. , 2021, , .		2
15	Fault Coexistence and Grading Aware TSV Test based on Delay Feature. International Journal of Circuits, Systems and Signal Processing, 2021, 15, 623-633.	0.3	0
16	Continuous-time Delta-Sigma Modulators: Single-loop versus MASH. , 2021, , .		1
17	LCHR-TSV: Novel Low Cost and Highly Repairable Honeycomb-Based TSV Redundancy Architecture for Clustered Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2938-2951.	2.7	55
18	Non-Intrusive Online Distributed Pulse Shrinking-Based Interconnect Testing in 2.5D IC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2657-2661.	3.0	40

#	Article	IF	Citations
19	CC-RTSV: Cross-Cellular Based Redundant TSV Design for 3D ICs. Journal of Circuits, Systems and Computers, 2020, 29, 2050144.	1.5	1
20	Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4684-4695.	5.4	50
21	Pattern Reorder for Test Cost Reduction Through Improved SVMRANK Algorithm. IEEE Access, 2020, 8, 147965-147972.	4.2	10
22	A low critical path delay structure for composite field AES S-box based on constant matrices multiplication merging. IEICE Electronics Express, 2020, 17, 20200035-20200035.	0.8	3
23	Architecture of Cobweb-Based Redundant TSV for Clustered Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1736-1739.	3.1	132
24	Information Assurance Through Redundant Design: A Novel TNU Error-Resilient Latch for Harsh Radiation Environment. IEEE Transactions on Computers, 2020, 69, 789-799.	3.4	66
25	A Sextuple Cross-Coupled SRAM Cell Protected against Double-Node Upsets. , 2020, , .		3
26	A Novel Built-In Self-Repair Scheme for 3D Memory. IEEE Access, 2019, 7, 65052-65059.	4.2	4
27	Temperature-Aware Floorplanning for Fixed-Outline 3D ICs. IEEE Access, 2019, 7, 139787-139794.	4.2	14
28	An enhanced time-to-digital conversion solution for pre-bond TSV dual faults testing. IEICE Electronics Express, 2019, 16, 20181105-20181105.	0.8	0
29	Novel approach of LSTM for adaptive testing. , 2019, , .		1
30	A Pulse Shrinking-Based Test Solution for Prebond Through Silicon via in 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 755-766.	2.7	17
31	An All-Digital and Jitter-Quantizing True Random Number Generator in SRAM-Based FPGAs. , 2018, , .		6
32	A Hybrid DMR Latch to Tolerate MNU Using TDICE and WDICE. , 2018, , .		2
33	Research on physical unclonable functions circuit based on three dimensional integrated circuit. IEICE Electronics Express, 2018, 15, 20180782-20180782.	0.8	3
34	A novel in-field TSV repair method for latent faults. IEICE Electronics Express, 2018, 15, 20180873-20180873.	0.8	2
35	A single event transient detector in SRAM-based FPGAs. IEICE Electronics Express, 2017, 14, 20170210-20170210.	0.8	5
36	Vernier ring based pre-bond through silicon vias test in 3D ICs. IEICE Electronics Express, 2017, 14, 20170590-20170590.	0.8	9

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37	A highly reliable butterfly PUF in SRAM-based FPGAs. IEICE Electronics Express, 2017, 14, 20170551-20170551.	0.8	11
38	A Region-Based Through-Silicon via Repair Method for Clustered Faults. IEICE Transactions on Electronics, 2017, E100.C, 1108-1117.	0.6	13
39	NBTI mitigation by M-IVC with input duty cycle and randomness constraints. , 2016, , .		0
40	Design of Radiation Hardened Latch and Flip-Flop with Cost-Effectiveness for Low-Orbit Aerospace Applications. Journal of Electronic Testing: Theory and Applications (JETTA), 0, , 1.	1.2	4