Naser Mohammadzadeh

List of Publications by Year
in descending order

32 papers	176 citations	1306789 7 h-index	1281420 11 g-index
32 all docs	32 docs citations	32 times ranked	89 citing authors

#	Article	IF	Citations
1	AMPS: An Automated Mesochronous Pipeline Scheduler and Design Space Explorer for High Performance Digital Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1681-1692.	3.5	2
2	A congestionâ€aware mixed integer linear programming model for placement and scheduling of quantum circuits with a twoâ€level heuristic solution approach. Quantum Engineering, 2021, 3, .	1.2	1
3	Automated window-based partitioning of quantum circuits. Physica Scripta, 2021, 96, 035102.	1.2	8
4	Exact Physical Design of Quantum Circuits for Ion-Trap-based Quantum Architectures. , 2021, , .		0
5	Efficient One-pass Synthesis for Digital Microfluidic Biochips. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-21.	1.9	0
6	A Transformation-Based Quantum Physical Synthesis Approach for Nearest-Neighbor Architectures. Quantum Reports, 2021, 3, 435-443.	0.6	1
7	Qubit mapping of one-way quantum computation patterns onto 2D nearest-neighbor architectures. Quantum Information Processing, 2019, 18, 1.	1.0	2
8	SAQIP. Transactions on Architecture and Code Optimization, 2019, 16, 1-21.	1.6	12
9	Mapping quantum circuits on 3D nearest-neighbor architectures. Quantum Science and Technology, 2019, 4, 035001.	2.6	6
10	The Lightweight Authentication Scheme with Capabilities of Anonymity and Trust in Internet of Things (IoT). Signal and Data Processing, 2019, 15, 111-122.	0.0	3
11	A powerâ€performance tunable logic with adjustable threshold pseudoâ€dynamic building blocks and <scp>CMOS</scp> compatibility. International Journal of Circuit Theory and Applications, 2018, 46, 796-811.	1.3	1
12	Quantum circuit physical design flow for <scp>2D</scp> nearestâ€neighbor architectures. International Journal of Circuit Theory and Applications, 2017, 45, 989-1000.	1.3	18
13	Physical synthesis of quantum circuits using templates. Quantum Information Processing, 2016, 15, 4117-4135.	1.0	5
14	Lightweight, anonymous and mutual authentication in IoT infrastructure. , 2016, , .		10
15	LDPC decoder implementation using FPGA. , 2016, , .		4
16	Physical design of quantum circuits in ion trap technology â€“ A survey. Microelectronics Journal, 2016, 55, 116-133.	1.1	7
17	Quantum circuit physical design flow for the multiplexed trap architecture. Microprocessors and Microsystems, 2016, 45, 23-31.	1.8	4
18	An MINLP Model for Scheduling and Placement of Quantum Circuits with a Heuristic Solution Approach. ACM Journal on Emerging Technologies in Computing Systems, 2015, 12, 1-20.	1.8	11

#	Article	IF	Citations
19	Optimal ILP-Based Approach for Gate Location Assignment and Scheduling in Quantum Circuits. Modelling and Simulation in Engineering, 2014, 2014, 1-8.	0.4	3
20	Quantum circuit physical design methodology with emphasis on physical synthesis. Quantum Information Processing, 2014, 13, 445-465.	1.0	13
21	A hierarchical layout generation method for quantum circuits. , 2013, , .		7
22	GATE LOCATION CHANGING: AN OPTIMIZATION TECHNIQUE FOR QUANTUM CIRCUITS. International Journal of Quantum Information, 2012, 10, 1250037.	0.6	6
23	Auxiliary qubit selection: a physical synthesis technique for quantum circuits. Quantum Information Processing, 2011, 10, 139-154.	1.0	12
24	Quantum physical synthesis: Improving physical design by netlist modifications. Microelectronics Journal, 2010, 41, 219-230.	1.1	18
25	Improving Latency of Quantum Circuits by Gate Exchanging. , 2009, , .		7
26	Multi-domain clock skew scheduling-aware register placement to optimize clock distribution network. , 2009, , .		5
27	The ODYSSEY approach to early simulation-based equivalence checking at ESL level using automatically generated executable transaction-level model. Microprocessors and Microsystems, 2008, 32, 364-374.	1.8	1
28	Evaluation and Improvement of Quantum Synthesis Algorithms based on a Thorough Set of Metrics. , 2008, , .		2
29	A FRAMEWORK FOR OBJECT-ORIENTED EMBEDDED SYSTEM DEVELOPMENT BASED ON OO-ASIPS. Journal of Circuits, Systems and Computers, 2008, 17, 973-993.	1.0	1
30	Implementation of a jpeg object-oriented ASIP. , 2007, , .		1
31	Using on-chip networks to implement polymorphism in the co-design of object-oriented embedded systems. Journal of Computer and System Sciences, 2007, 73, 1221-1231.	0.9	1
32	Software Implementation of MPEG2 Decoder on an ASIP JPEG Processor. , 0, , .		4