Vijaykrishnan Narayanan

List of Publications by Year
in descending order

129	2,666	361045	301761
papers	citations	20 h-index	39 g-index

132	132	132	2014
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Effective Capacitance and Drive Current for Tunnel FET (TFET) CV/I Estimation. IEEE Transactions on Electron Devices, 2009, 56, 2092-2098.	1.6	197
2	On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors. IEEE Electron Device Letters, 2009, 30, 1102-1104.	2.2	188
3	Synchronized charge oscillations in correlated electron systems. Scientific Reports, 2014, 4, .	1.6	155
4	Design and evaluation of a hierarchical on-chip interconnect for next-generation CMPs. , 2009, , .		135
5	Variation-tolerant ultra low-power heterojunction tunnel FET SRAM design. , 2011, , .		114
6	Nonvolatile memory design based on ferroelectric FETs. , 2016, , .		91
7	Device-Circuit Analysis of Ferroelectric FETs for Low-Power Logic. IEEE Transactions on Electron Devices, 2017, 64, 3092-3100.	1.6	86
8	Toward Increasing FPGA Lifetime. IEEE Transactions on Dependable and Secure Computing, 2008, 5, 115-127.	3.7	73
9	Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET. IEEE Transactions on Electron Devices, 2017, 64, 3452-3458.	1.6	72
10	Tunnel FET RF Rectifier Design for Energy Harvesting Applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 400-411.	2.7	70
11	Analysis of DIBL Effect and Negative Resistance Performance for NCFET Based on a Compact SPICE Model. IEEE Transactions on Electron Devices, 2018, 65, 5525-5529.	1.6	57
12	A low-power phase change memory based hybrid cache architecture. , 2008, , .		51
13	On the Effects of Process Variation in Network-on-Chip Architectures. IEEE Transactions on Dependable and Secure Computing, 2010, 7, 240-254.	3.7	50
14	Advancing Nonvolatile Computing With Nonvolatile NCFET Latches and Flip-Flops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2907-2919.	3.5	49
15	Design of Nonvolatile SRAM with Ferroelectric FETs for Energy-Efficient Backup and Restore. IEEE Transactions on Electron Devices, 2017, 64, 3037-3040.	1.6	48
16	Steep switching tunnel FET: A promise to extend the energy efficient roadmap for post-CMOS digital and analog/RF applications. , 2013, , .		46
17	Soft-Error Performance Evaluation on Emerging Low Power Devices. IEEE Transactions on Device and Materials Reliability, 2014, 14, 732-741.	1.5	45
18	Designing a 3-D FPGA: Switch Box Architecture and Thermal Issues. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 882-893.	2.1	40

#	Article	IF	Citations
19	Utilization of Negative-Capacitance FETs to Boost Analog Circuit Performances. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2855-2860.	2.1	40
20	Influence of Body Effect on Sample-and-Hold Circuit Design Using Negative Capacitance FET. IEEE Transactions on Electron Devices, 2018, 65, 3909-3914.	1.6	38
21	Device Circuit Co Design of FEFET Based Logic for Low Voltage Processors. , 2016, , .		35
22	Rf-powered systems using steep-slope devices. , 2014, , .		34
23	A Hardware Efficient Support Vector Machine Architecture for FPGA. , 2008, , .		33
24	GaaS-X: Graph Analytics Accelerator Supporting Sparse Data Representation using Crossbar Architectures. , 2020, , .		31
25	Compact 3-D-SRAM Memory With Concurrent Row and Column Data Access Capability Using Sequential Monolithic 3-D Integration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 671-683.	2.1	28
26	An FPGA Implementation of Information Theoretic Visual-Saliency System and Its Optimization. , 2011, , .		27
27	A Steep-Slope Tunnel FET Based SAR Analog-to-Digital Converter. IEEE Transactions on Electron Devices, 2014, 61, 3661-3667.	1.6	27
28	Tunnel FET-based ultra-low power, high-sensitivity UHF RFID rectifier. , 2013, , .		26
29	Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. IEEE Design and Test, 2019, 36, 39-45.	1.1	26
30	Mismatch of Ferroelectric Film on Negative Capacitance FETs Performance. IEEE Transactions on Electron Devices, 2020, 67, 1297-1304.	1.6	26
31	Emerging reconfigurable nanotechnologies. , 2018, , .		25
32	TSV-free FinFET-based Monolithic 3D⁺-IC with computing-in-memory SRAM cell for intelligent IoT devices. , 2017, , .		24
33	NEBULA: A Neuromorphic Spin-Based Ultra-Low Power Architecture for SNNs and ANNs. , 2020, , .		23
34	Emulating Mammalian Vision on Reconfigurable Hardware. , 2012, , .		22
35	FPGA Architecture for 2D Discrete Fourier Transform Based on 2D Decomposition for Large-sized Data. Journal of Signal Processing Systems, 2011, 64, 109-122.	1.4	21
36	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, 2018, 65, 2670-2674.	1.6	21

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37	Process-Variation-Aware Adaptive Cache Architecture and Management. IEEE Transactions on Computers, 2009, 58, 865-877.	2.4	20
38	Multidimensional DFT IP Generator for FPGA Platforms. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 755-764.	3.5	20
39	Thermal-aware reliability analysis for Platform FPGAs. , 2008, , .		19
40	Nonvolatile processors: Why is it trending?. , 2017, , .		19
41	A reconfigurable accelerator for neuromorphic object recognition. , 2012, , .		18
42	Spendthrift: Machine learning based resource and frequency scaling for ambient energy harvesting nonvolatile processors. , 2017, , .		18
43	Dynamic Power and Energy Management for Energy Harvesting Nonvolatile Processor Systems. Transactions on Embedded Computing Systems, 2017, 16, 1-23.	2.1	18
44	Improving energy efficiency of multi-threaded applications using heterogeneous CMOS-TFET multicores. , 2011, , .		16
45	Dynamic machine learning based matching of nonvolatile processor microarchitecture to harvested energy profile. , 2015, , .		16
46	ROBIN: Monolithic-3D SRAM for Enhanced Robustness with In-Memory Computation Support. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2533-2545.	3.5	16
47	Design of Thermally Robust Clock Trees Using Dynamically Adaptive Clock Buffers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 374-383.	3.5	15
48	Symmetric 2-D-Memory Access to Multidimensional Data. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1040-1050.	2.1	15
49	A Unified Streaming Architecture for Real Time Face Detection and Gender Classification. , 2007, , .		14
50	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface. , 2020, , .		14
51	System-On-Chip for Biologically Inspired Vision Applications. IPSJ Transactions on System LSI Design Methodology, 2012, 5, 71-95.	0.5	13
52	Optimizing the NoC Slack Through Voltage and Frequency Scaling in Hard Real-Time Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1632-1643.	1.9	13
53	A Monolithic-3D SRAM Design with Enhanced Robustness and In-Memory Computation Support. , 2018, , .		13
54	Accelerating the Nonuniform Fast Fourier Transform Using FPGAs. , 2010, , .		12

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55	On Reconfigurable Single-Electron Transistor Arrays Synthesis Using Reordering Techniques. , 2013, , .		12
56	Monolithic-3D Integration Augmented Design Techniques for Computing in SRAMs. , 2019, , .		12
57	SHARC: A streaming model for FPGA accelerators and its application to Saliency. , 2011, , .		11
58	TS-Router: On maximizing the Quality-of-Allocation in the On-Chip Network. , 2013, , .		11
59	A Reconfigurable Low-Power BDD Logic Architecture Using Ferroelectric Single-Electron Transistors. IEEE Transactions on Electron Devices, 2015, 62, 1052-1057.	1.6	10
60	Correlated Material Enhanced SRAMs With Robust Low Power Operation. IEEE Transactions on Electron Devices, 2016, 63, 4744-4752.	1.6	10
61	MDACache: Caching for Multi-Dimensional-Access Memories. , 2018, , .		10
62	Exploring Gabor Filter Implementations for Visual Cortex Modeling on FPGA. , 2011, , .		9
63	When to forget: A system-level perspective on STT-RAMs. , 2012, , .		9
64	Low-power high-speed current mode logic using Tunnel-FETs. , 2014, , .		9
65	Design of energyâ€efficient circuits and systems using tunnel field effect transistors. IET Circuits, Devices and Systems, 2013, 7, 294-303.	0.9	8
66	AIGuide: An Augmented Reality Hand Guidance Application for People with Visual Impairments. , 2020, , .		8
67	ShieldUS: A novel design of dynamic shielding for eliminating 3D TSV crosstalk coupling noise. , 2013, , .		7
68	Single-Ended and Differential MRAMs Based on Spin Hall Effect: A Layout-Aware Design Perspective. , 2015, , .		7
69	Ultra-Low Power 3D NC-FinFET-based Monolithic 3D⁺ -IC with Computing-in-Memory for Intelligent IoT Devices. , 2018, , .		7
70	Byzantine-Tolerant Inference in Distributed Deep Intelligent System: Challenges and Opportunities. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 509-519.	2.7	7
71	FPGA architecture for 2D Discrete Fourier Transform based on 2D decomposition for large-sized data. , 2009, , .		6
72	Exploration of Low-Power High-SFDR Current-Steering D/A Converter Design Using Steep-Slope Heterojunction Tunnel FETs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-11.	2.1	6

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73	Improving FPGA Design with Monolithic 3D Integration Using High Dense Inter-Stack Via. , 2017, , .		6
74	A FerroFET-Based In-Memory Processor for Solving Distributed and Iterative Optimizations via Least-Squares Method. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 132-141.	1.1	6
75	SRAMs and DRAMs With Separate Readâ€“Write Ports Augmented by Phase Transition Materials. IEEE Transactions on Electron Devices, 2019, 66, 929-937.	1.6	6
76	FARM: A Flexible Accelerator for Recurrent and Memory Augmented Neural Networks. Journal of Signal Processing Systems, 2020, 92, 1247-1261.	1.4	6
77	Gesture-SNN: Co-optimizing accuracy, latency and energy of SNNs for neuromorphic vision sensors. , 2021, , .		6
78	Design Space Exploration of Ferroelectric Tunnel Junction Toward Crossbar Memories. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 115-122.	1.1	6
79	Hardware functional obfuscation with ferroelectric active interconnects. Nature Communications, 2022, 13, 2235.	5.8	6
80	Bandwidth-intensive FPGA architecture for multi-dimensional DFT. , 2010, , .		5
81	Towards Resilient Micro-architectures: Datapath Reliability Enhancement Using STT-MRAM. , 2011, , .		5
82	Synthesis for Width Minimization in the Single-Electron Transistor Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2862-2875.	2.1	5
83	Co-training of Feature Extraction and Classification using Partitioned Convolutional Neural Networks. , 2017, , .		5
84	Programmable Non-Volatile Memory Design Featuring Reconfigurable In-Memory Operations. , 2019, , .		5
85	An Automated Framework for Accelerating Numerical Algorithms on Reconfigurable Platforms Using Algorithmic/Architectural Optimization. IEEE Transactions on Computers, 2009, 58, 1654-1667.	2.4	4
86	Harnessing Emerging Technology for Compute-in-Memory Support. , 2018, , .		4
87	Integrated CAM-RAM Functionality using Ferroelectric FETs. , 2020, , .		4
88	A criticality-driven microarchitectural three dimensional (3D) floorplanner. , 2009, , .		3
89	Lifetime Reliability Aware Design Flow Techniques for Dual-Vdd Based Platform FPGAs. , 2009, , .		3
90	Optimizing power and performance for reliable on-chip networks. , 2010, , .		3

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91	FPGA-accelerator system for computing biologically inspired feature extraction models. , 2011, , .		3
92	Saliency-driven dynamic configuration of HMAX for energy-efficient multi-object recognition. , 2013, , .		3
93	Exploring memory controller configurations for many-core systems with 3D stacked DRAMs. , 2015, , .		3
94	Diagnosis and Synthesis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, , 1-14.	2.1	3
95	One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3402-3406.	2.2	3
96	Trends and Opportunities for SRAM Based In-Memory and Near-Memory Computation. , 2021, , .		3
97	A Real Time Embedded Face Detector on FPGA. , 2006, , .		2
98	Analyzing Energy-Delay Behavior in Room Temperature Single Electron Transistors. , 2010, , .		2
99	Impact of Circuit Degradation on FPGA Design Security. , 2011, , .		2
100	Multiresolution Gabor Feature Extraction for Real Time Applications. , 2012, , .		2
101	Width minimization in the Single-Electron Transistor array synthesis. , 2014, , .		2
102	A Low-Voltage Low-Power LC Oscillator Using the Diode-Connected SymFET. , 2014, , .		2
103	Dynamic Diagnosis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1477-1489.	2.1	2
104	A Power-Efficient Hybrid Architecture Design for Image Recognition Using CNNs. , 2018, , .		2
105	Technology-Assisted Computing-In-Memory Design for Matrix Multiplication Workloads. , 2019, , .		2
106	CiM3D: Comparator-in-Memory Designs Using Monolithic 3-D Technology for Accelerating Data-Intensive Applications. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 79-87.	1.1	2
107	DyTAN: Dynamic Ternary Content Addressable Memory Using Nanoelectromechanical Relays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1981-1993.	2.1	2
108	Width minimization in the Single-Electron Transistor array synthesis. , 2014, , .		2

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109	An FPGA-based accelerator for cortical object classification. , 2012, , .		1
110	A reconfigurable platform for the design and verification of domain-specific accelerators. , 2012, , .		1
111	A Saliency-Driven LCD Power Management System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2689-2702.	2.1	1
112	Heuristic Approximation of Early-Stage CNN Data Representation for Vision Intelligence Systems. , 2018, , .		1
113	Indoor Navigation using Text Extraction. , 2018, , .		1
114	Adaptive Neural Network Architectures for Power Aware Inference. IEEE Design and Test, 2020, 37, 66-75.	1.1	1
115	Optimization of Intercache Traffic Entanglement in Tagless Caches With Tiling Opportunities. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3881-3892.	1.9	1
116	Resolution-Aware Deep Multi-View Camera Systems. , 2021, , .		1
117	Microprocessor at 50: Industry Leaders Speak. IEEE Micro, 2021, 41, 13-15.	1.8	1
118	Power efficient adaptive M-QAM design using adaptive pipelined analog-to-digital converter. , 2002, , .		0
119	Power and area reduction using carbon nanotube bundle interconnect in global clock tree distribution network. , 2009, , .		0
120	Invited paper: Accelerating neuromorphic vision on FPGAs. , 2011, , .		0
121	Hazard driven test generation for SMT processors. , 2012, , .		0
122	A Configurable Architecture for a Visual Saliency System and Its Application in Retail. , 2013, , .		0
123	Data driven adaptation for QoS aware embedded vision systems. , 2014, , .		0
124	Intelligent Vision Systems: Exploring the State-of-the-Art and Opportunities for the Future. , 2015, , .		0
125	Towards a unified multiresolution vision model for autonomous ground robots. Robotics and Autonomous Systems, 2016, 75, 221-232.	3.0	0
126	Monolithic 3D Enabled Processing-in- SRAM Memory. , 2020, , .		0

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127	Microprocessor at 50: A Time to Celebrate and Energize for the Future. IEEE Micro, 2021, 41, 10-12.	1.8	0
128	Intel Wins in Four Decades, but AMD Catches Up. IEEE Micro, 2021, 41, 168-171.	1.8	0
129	Sparse Vector-Matrix Multiplication Acceleration in Diode-Selected Crossbars. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2186-2196.	2.1	0