Chi-Hang Chan

List of Publications by Year
in descending order

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49 papers	1,331 citations	516710 16 h-index	361022 35 g-index
49 all docs	49 docs citations	49 times ranked	760 citing authors

#	Article	IF	Citations
1	A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1111-1121.	5.4	571
2	A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration. IEEE Journal of Solid-State Circuits, 2018, 53, 850-860.	5.4	55
3	A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 322-332.	5.4	43
4	A reconfigurable low-noise dynamic comparator with offset calibration in 90nm CMOS. , 2011, , .		40
5	60-dB SNDR 100-MS/s SAR ADCs With Threshold Reconfigurable Reference Error Calibration. IEEE Journal of Solid-State Circuits, 2017, 52, 2576-2588.	5.4	40
6	A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC. IEEE Journal of Solid-State Circuits, 2016, 51, 365-377.	5.4	32
7	A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques. IEEE Journal of Solid-State Circuits, 2019, 54, 3396-3409.	5.4	32
8	An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2016, 51, 1223-1234.	5.4	30
9	An 8-Bit 10-GS/s 16Ã— Interpolation-Based Time-Domain ADC With <1.5-ps Uncalibrated Quantization Steps. IEEE Journal of Solid-State Circuits, 2020, 55, 3225-3235.	5.4	30
10	A 50-fJ 10-b 160-MS/s Pipelined-SAR ADC Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation. IEEE Journal of Solid-State Circuits, 2012, 47, 2614-2626.	5.4	27
11	A 7-bit 2 GS/s Time-Interleaved SAR ADC With Timing Skew Calibration Based on Current Integrating Sampler. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 557-568.	5.4	27
12	Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1203-1207.	3.1	24
13	A 12b 180MS/s 0.068mm² With Full-Calibration-Integrated Pipelined-SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1684-1695.	5.4	24
14	16.4 A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration. , 2017, , .		21
15	A 7.8-mW 5-b 5-GS/s Dual-Edges-Triggered Time-Based Flash ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1966-1976.	5.4	21
16	Passive Noise Shaping in SAR ADC With Improved Efficiency. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 416-420.	3.1	21
17	A 34fJ 10b 500 MS/s partial-interleaving pipelined SAR ADC. , 2012, , .		20
18	A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2154-2169.	5.4	18

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19	A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC. IEEE Journal of Solid-State Circuits, 2020, 55, 312-321.	5.4	16
20	A 2nd-Order Noise-Shaping SAR ADC With Lossless Dynamic Amplifier Assisted Integrator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1819-1823.	3.0	16
21	A 89fJ-FOM 6-bit 3.4GS/s flash ADC with 4x time-domain interpolation. , 2015, , .		14
22	Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2603-2607.	3.1	14
23	A 5.35-mW 10-MHz Single-Opamp Third-Order CT <inline-formula> <tex-math notation="LaTeX">$DeltaSigma$ </tex-math> </inline-formula> Modulator With CTC Amplifier and Adaptive Latch DAC Driver in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2783-2794.	5.4	13
24	An 11b 900 MS/s time-interleaved sub-ranging pipelined-SAR ADC. , 2014, , .		12
25	Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial $V_{mathrm {cm}}$ -Based Switching. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1168-1172.	3.1	12
26	A 0.19 mm² 10 b 2.3 GS/s 12-Way Time-Interleaved Pipelined-SAR ADC in 65-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3606-3616.	5.4	12
27	Analysis of Reference Error in High-Speed SAR ADCs With Capacitive DAC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 82-93.	5.4	10
28	Accuracy-Enhanced Variance-Based Time-Skew Calibration Using SAR as Window Detector. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 481-485.	3.1	10
29	16.2 A 4Ã— Interleaved 10GS/s 8b Time-Domain ADC with 16Ã— Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input. , 2020, , .		10
30	A 40-MHz Bandwidth 75-dB SNDR Partial-Interleaving SAR-Assisted Noise-Shaping Pipeline ADC. IEEE Journal of Solid-State Circuits, 2021, 56, 1772-1783.	5.4	10
31	16.3 A â˜’246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT. , 2019, , .		9
32	An 11-bit 100-MS/s Pipelined-SAR ADC Reusing PVT-Stabilized Dynamic Comparator in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1174-1178.	3.0	9
33	A 0.04% BER Strong PUF With Cell-Bias-Based CRPs Filtering and Background Offset Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3853-3865.	5.4	8
34	A 3.3-GS/s 6-b Fully Dynamic Pipelined ADC With Linearized Dynamic Amplifier. IEEE Journal of Solid-State Circuits, 2022, 57, 1673-1683.	5.4	8
35	Analysis of Common-Mode Interference and Jitter of Clock Receiver Circuits With Improved Topology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1819-1829.	5.4	7
36	A Calibration-Free Ring-Oscillator PLL With Gain Tracking Achieving 9% Jitter Variation Over PVT. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3753-3763.	5.4	7

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37	Bird'sâ€eye view of analog and mixedâ€signal chips for the 21st century. International Journal of Circuit Theory and Applications, 2021, 49, 746-761.	2.0	7
38	A 20 MHz Bandwidth 79 dB SNDR SAR-Assisted Noise-Shaping Pipeline ADC With Gain and Offset Calibrations. IEEE Journal of Solid-State Circuits, 2022, 57, 745-756.	5.4	7
39	A 2-GS/s 8-Bit ADC Featuring Virtual-Ground Sampling Interleaved Architecture in 28-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1534-1538.	3.0	6
40	Background Offset Calibration for Comparator Based on Temperature Drift Profile. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1648-1652.	3.0	5
41	A 100-MHz BW 72.6-dB-SNDR CT Î” Î£ Modulator Utilizing Preliminary Sampling and Quantization. IEEE Journal of Solid-State Circuits, 2020, , 1-1.	5.4	5
42	A Single-Opamp Third Order CT Î”Î£ Modulator With SAB-ELD-Merged Integrator and Three-Stage Hybrid Compensation Opamp. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 64-74.	5.4	5
43	A 7b 2 GS/s Time-Interleaved SAR ADC with Time Skew Calibration Based on Current Integrating Sampler. , 2018, , .		4
44	Missing-Code-Occurrence Probability Calibration Technique for DAC Nonlinearity With Supply and Reference Circuit Analysis in a SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3707-3719.	5.4	4
45	An Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC With Code-Counter-Based Offset Calibration. IEEE Journal of Solid-State Circuits, 2022, 57, 1480-1491.	5.4	4
46	Gain Error Calibrations for Two-Step ADCs: Optimizations Either in Accuracy or Chip Area. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2279-2289.	3.1	3
47	Design of a High-Speed Time-Interleaved Sub-Ranging SAR ADC With Optimal Code Transfer Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 489-501.	5.4	3
48	A 65.5-dB SNDR 8.1â€“11.1-nW ECG SAR ADC With Adaptive-Latching OSC-Based Comparator and DAC Calibration. IEEE Solid-State Circuits Letters, 2020, 3, 482-485.	2.0	3
49	A 4-b 7-mu W Phase Domain ADC With Time Domain Reference Generation for Low-Power FSK/PSK Demodulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3365-3372.	5.4	2