Wenjie Xiong

List of Publications by Year
in descending order

16 papers	222 citations	1478505 6 h-index	1588992 8 g-index
17 all docs	17 docs citations	17 times ranked	115 citing authors

#	Article	IF	Citations
1	Run-Time Accessible DRAM PUFs in Commodity Devices. Lecture Notes in Computer Science, 2016, , 432-453.	1.3	37
2	Intrinsic Rowhammer PUFs: Leveraging the Rowhammer effect for improved security. , 2017, , .		35
3	Decay-Based DRAM PUFs in Commodity Devices. IEEE Transactions on Dependable and Secure Computing, 2019, 16, 462-475.	5.4	34
4	Analysis of Secure Caches Using a Three-Step Model for Timing-Based Attacks. Journal of Hardware and Systems Security, 2019, 3, 397-425.	1.3	18
5	Survey of Transient Execution Attacks and Their Mitigations. ACM Computing Surveys, 2022, 54, 1-36.	23.0	18
6	Cache timing side-channel vulnerability checking with computation tree logic. , 2018, , .		17
7	Secure TLBs. , 2019, , .		13
8	Spying on Temperature using DRAM. , 2019, , .		10
9	Intrinsic Run-Time Row Hammer PUFs: Leveraging the Row Hammer Effect for Run-Time Cryptography and Improved Security â€. Cryptography, 2018, 2, 13.	2.3	9
10	A Benchmark Suite for Evaluating Caches' Vulnerability to Timing Attacks. , 2020, , .		9
11	Leaking Information Through Cache LRU States in Commercial Processors and Secure Caches. IEEE Transactions on Computers, 2021, 70, 511-523.	3.4	8
12	Software Protection Using Dynamic PUFs. IEEE Transactions on Information Forensics and Security, 2020, 15, 2053-2068.	6.9	5
13	Dynamic Physically Unclonable Functions. , 2019, , .		4
14	Evaluation of Cache Attacks on Arm Processors and Secure Caches. IEEE Transactions on Computers, 2021, , 1-1.	3.4	4
15	Understanding the Insecurity of Processor Caches Due to Cache Timing-Based Vulnerabilities. IEEE Security and Privacy, 2021, 19, 42-49.	1.2	0
16	DRAM PUFs in Commodity Devices. IEEE Design and Test, 2021, 38, 76-83.	1.2	0