Srinivas Katkoori

List of Publications by Year
in descending order

86	1,306	759055 12	526166 27
papers	citations	h-index	g-index

89	89	89	817
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Point & Teleport Locomotion Technique for Virtual Reality. , 2016, , .		278
2	Selective triple Modular redundancy (STMR) based single-event upset (SEU) tolerant synthesis for FPGAs. IEEE Transactions on Nuclear Science, 2004, 51, 2957-2969.	1.2	158
3	A genetic algorithm for the design space exploration of datapaths during high-level synthesis. IEEE Transactions on Evolutionary Computation, 2006, 10, 213-229.	7.5	98
4	A Survey on Virtual Reality for Individuals with Autism Spectrum Disorder: Design Considerations. IEEE Transactions on Learning Technologies, 2018, 11, 133-151.	2.2	89
5	Customizable FPGA IP Core Implementation of a General-Purpose Genetic Algorithm Engine. IEEE Transactions on Evolutionary Computation, 2010, 14, 133-149.	7.5	67
6	Locomotion in virtual reality for room scale tracked areas. International Journal of Human Computer Studies, 2019, 122, 38-49.	3.7	57
7	Vocational Rehabilitation of Individuals with Autism Spectrum Disorder with Virtual Reality. ACM Transactions on Accessible Computing, 2017, 10, 1-25.	1.9	41
8	A Framework for Power-Gating Functional Units in Embedded Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1640-1649.	2.1	37
9	Locomotion in Virtual Reality for Individuals with Autism Spectrum Disorder. , 2016, , .		34
10	A novel method for watermarking sequential circuits. , 2012, , .		30
11	CSRO-Based Reconfigurable True Random Number Generator Using RRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2661-2670.	2.1	29
12	Power minimization algorithms for LUT-based FPGA technology mapping. ACM Transactions on Design Automation of Electronic Systems, 2004, 9, 33-51.	1.9	24
13	State-Retentive Power Gating of Register Files in Multicore Processors Featuring Multithreaded In-Order Cores. IEEE Transactions on Computers, 2011, 60, 1547-1560.	2.4	20
14	Design, Analysis and Application of Embedded Resistive RAM Based Strong Arbiter PUF. IEEE Transactions on Dependable and Secure Computing, 2020, 17, 1232-1242.	3.7	20
15	Knapbind: an area-efficient binding algorithm for low-leakage datapaths. , 0, , .		17
16	An Elitist Non-Dominated Sorting Based Genetic Algorithm for Simultaneous Area and Wirelength Minimization in VLSI Floorplanning. , 2008, , .		16
17	Net-based force-directed macrocell placement for wirelength optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 824-835.	2.1	13
18	High-Level Synthesis of Key-Obfuscated RTL IP with Design Lockout and Camouflaging. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-35.	1.9	13

#	Article	IF	Citations
19	Embedded system design of a real-time parking guidance system. , 2016, , .		12
20	Simultaneous Scheduling, Allocation, Binding, Re-Ordering, and Encoding for Crosstalk Pattern Minimization During Highâ€“Level Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 217-226.	2.1	11
21	LSTM-Based Memory Profiling for Predicting Data Attacks in Distributed Big Data Systems. , 2017, , .		11
22	High-level synthesis of key based obfuscated RTL datapaths. , 2018, , .		11
23	Machine Learning Based IoT Edge Node Security Attack and Countermeasures. , 2019, , .		11
24	A Compiler Based Leakage Reduction Technique by Power-Gating Functional Units in Embedded Microprocessors. , 2007, , .		10
25	Effects of Virtual Reality Properties on User Experience of Individuals with Autism. ACM Transactions on Accessible Computing, 2018, 11, 1-27.	1.9	10
26	Vocational training with immersive virtual reality for individuals with autism: towards better design practices. , 2016, , .		9
27	Virtual Reality Interaction Techniques for Individuals with Autism Spectrum Disorder: Design Considerations and Preliminary Results. Lecture Notes in Computer Science, 2016, , 127-137.	1.0	9
28	Architectural Power Estimation Based on Behavior Level Profiling. VLSI Design, 1998, 7, 255-270.	0.5	9
29	Novel Bit-Sliced Near-Memory Computing Based VLSI Architecture for Fast Sobel Edge Detection in IoT Edge Devices. , 2020, , .		9
30	An efficient register optimization algorithm for high-level synthesis from hierarchical behavioral specifications. ACM Transactions on Design Automation of Electronic Systems, 2002, 7, 189-216.	1.9	8
31	A customizable FPGA IP core implementation of a general purpose Genetic Algorithm engine. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	7
32	Clock Period Minimization with Iterative Binding Based on Stochastic Wirelength Estimation during High-Level Synthesis. , 2008, , .		7
33	Fast Sobel Edge Detection for IoT Edge Devices. SN Computer Science, 2022, 3, .	2.3	7
34	A 3D-Layout Aware Binding Algorithm for High-Level Synthesis of Three-Dimensional Integrated Circuits. , 2007, , .		6
35	Floorplan Driven High Level Synthesis for Crosstalk Noise Minimization in Macro-cell Based Designs. , 2009, , .		6
36	TABS: Temperature-Aware Layout-Driven Behavioral Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1649-1659.	2.1	6

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37	Empirical Word-Level Analysis of Arithmetic Module Architectures for Hardware Trojan Susceptibility. , 2018, , .		6
38	A Framework for Hardware Trojan Vulnerability Estimation and Localization in RTL Designs. Journal of Hardware and Systems Security, 2020, 4, 246-262.	0.8	6
39	Virtual Reality Interaction Techniques for Individuals with Autism Spectrum Disorder. Lecture Notes in Computer Science, 2018, , 58-77.	1.0	6
40	Self-Reconfigurable Analog Array Integrated Circuit Architecture for Space Applications. , 2008, , .		5
41	On-chip dynamic worst-case crosstalk pattern detection and elimination for bus-based macro-cell designs. , 2009, , .		5
42	Embedded system design of an advanced illumination measurement system for highways. , 2014, , .		5
43	Minimizing Performance and Energy Overheads Due to Fanout In Memristor based Logic Implementations. , 2018, , .		5
44	Optimizing Performance and Energy Overheads Due to Fanout in In-Memory Computing Systems. IFIP Advances in Information and Communication Technology, 2019, , 147-166.	0.5	5
45	Simultaneous Peak Temperature and Average Power Minimization during Behavioral Synthesis. , 2009, , .		4
46	An Efficient Hardware-Oriented Runtime Approach for Stack-based Software Buffer Overflow Attacks. , 2018, , .		4
47	An SR Flip-Flop based Physical Unclonable Functions for Hardware Security. , 2019, , .		4
48	Gate Level NBTI and Leakage Co-Optimization in Combinational Circuits with Input Vector Cycling. IEEE Transactions on Emerging Topics in Computing, 2020, 8, 738-749.	3.2	4
49	Simultaneous Scheduling, Allocation, Binding, Re-ordering, and Encoding for Crosstalk Pattern Minimization during High Level Synthesis. , 2008, , .		3
50	Compiler-directed leakage reduction in embedded microprocessors. , 2009, , .		3
51	Self similarity and interval arithmetic based leakage optimization in RTL datapaths. , 2014, , .		3
52	Design and implementation of an embedded system for monitoring at-home solitary Alzheimer's patients. , 2015, , .		3
53	A Darwinian Genetic Algorithm for State Encoding Based Finite State Machine Watermarking. , 2019, , .		3
54	Variable Record Table: A Run-time Solution for Mitigating Buffer Overflow Attack. , 2019, , .		3

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55	Extreme Temperature Electronics based on Self-Adaptive System using Field Programmable Gate Array. , 2007, , .		2
56	Temperature-Adaptive Circuits on Reconfigurable Analog Arrays. , 2007, , .		2
57	Interval arithmetic based input vector control for RTL subthreshold leakage minimization. , 2012, , .		2
58	Interval arithmetic based input vector control for RTL subthreshold leakage minimization. , 2012, , .		2
59	State encoding based NBTI optimization in finite state machines. , 2016, , .		2
60	Analysis of Radiation Impact on Memristive Crossbar Arrays. , 2020, , .		2
61	Analytical Estimation and Localization of Hardware Trojan Vulnerability in RTL Designs. , 2020, , .		2
62	Net Clustering Based Constructive and Iterative Improvement Approaches for Macro-Cell Placement. Journal of Signal Processing Systems, 2004, 37, 151-163.	1.0	1
63	Bus Binding, Re-ordering, and Encoding for Crosstalk-Producing Switching Activity Minimization during High Level Synthesis. , 2008, , .		1
64	Exploring compiler optimizations for enhancing power gating. , 2009, , .		1
65	Memory access pattern based insider threat detection in big data systems. , 2016, , .		1
66	DLockout: A Design Lockout Technique for Key Obfuscated RTL IP Designs. , 2019, , .		1
67	High Level Modeling of Memristive Crossbar Arrays. , 2020, , .		1
68	SafeController: Efficient and Transparent Control-Flow Integrity for RTL Design. , 2020, , .		1
69	Machine Learning Attacks and Countermeasures for PUF-Based IoT Edge Node Security. SN Computer Science, 2020, 1, 1.	2.3	1
70	Partial evaluation based triple modular redundancy for single event upset mitigation. The Integration VLSI Journal, 2021, 77, 167-179.	1.3	1
71	Adaptive and Evolvable Analog Electronics for Space Applications. Lecture Notes in Computer Science, 2007, , 379-390.	1.0	1
72	Self-Reconfigurable Mixed-Signal Integrated Circuits Architecture Comprising a Field Programmable Analog Array and a General Purpose Genetic Algorithm IP Core. Lecture Notes in Computer Science, 0, , 225-236.	1.0	1

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73	Basic Block Encoding Based Run-time CFI Check for Embedded Software. , 2020, , .		1
74	Early Design Space Exploration Framework for Memristive Crossbar Arrays. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-26.	1.8	1
75	Minimizing wire delays by net-topology aware binding during floorplan- driven high level synthesis. , 2007, , .		0
76	"Glitch Logic" and Applications to Computing and Information Security. , 2009, , .		0
77	Pneumatically Actuated Diaphragm Single Chamber Micropump. , 2010, , .		0
78	A novel approach to crosstalk noise analysis in CMOS inverter driven coupled RLC interconnects. , 2013, , .		0
79	Overcoming Fitness, Symptom, And Behavior Barriers After A Physical Activity Intervention With Fitness Graded Motion Exergames (PAfitME) Among Head And Neck Cancer Patients. Medicine and Science in Sports and Exercise, 2019, 51, 899-899.	0.2	0
80	A Smart IoT System for Continuous Sleep State Monitoring. , 2020, , .		0
81	Defending Against Misspeculation-based Cache Probe Attacks Using Variable Record Table. , 2021, , .		0
82	RT-Level Route-and-Place Design Methodology for Interconnect Optimization in DSM Regime. IFIP Advances in Information and Communication Technology, 2000, , 427-438.	0.5	0
83	Interval Arithmetic and Self Similarity Based Subthreshold Leakage Optimization in RTL Datapaths. IFIP Advances in Information and Communication Technology, 2015, , 75-94.	0.5	0
84	Interval Arithmetic and Self-Similarity Based RTL Input Vector Control for Datapath Leakage Minimization. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-26.	1.9	0
85	Hardware Trojan Localization: Modeling and Empirical Approach. , 2022, , 205-231.		0
86	State Encoding Based Watermarking of Sequential Circuits Using Hybridized Darwinian Genetic Algorithm. , 2022, , 177-202.		0