

# Soochang Lee

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/6010417/publications.pdf>

Version: 2024-02-01

18  
papers

242  
citations

1307594

7  
h-index

996975

15  
g-index

18  
all docs

18  
docs citations

18  
times ranked

184  
citing authors

#	ARTICLE	IF	CITATIONS
1	Emerging memory technologies for neuromorphic computing. <i>Nanotechnology</i> , 2019, 30, 032001.	2.6	62
2	Demonstration of Unsupervised Learning With Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array. <i>IEEE Transactions on Electron Devices</i> , 2018, 65, 1774-1780.	3.0	54
3	A Split-Gate Positive Feedback Device With an Integrate-and-Fire Capability for a High-Density Low-Power Neuron Circuit. <i>Frontiers in Neuroscience</i> , 2018, 12, 704.	2.8	24
4	3-D AND-Type Flash Memory Architecture With High- $\epsilon_r$ Gate Dielectric for High-Density Synaptic Devices. <i>IEEE Transactions on Electron Devices</i> , 2021, 68, 3801-3806.	3.0	16
5	Unsupervised online learning of temporal information in spiking neural network using thin-film transistor-type NOR flash memory devices. <i>Nanotechnology</i> , 2019, 30, 435206.	2.6	13
6	Hardware-based spiking neural network architecture using simplified backpropagation algorithm and homeostasis functionality. <i>Neurocomputing</i> , 2021, 428, 153-165.	5.9	12
7	A Spiking Neural Network with a Global Self-Controller for Unsupervised Learning Based on Spike-Timing-Dependent Plasticity Using Flash Memory Synaptic Devices. , 2019, , .		9
8	SiO <sub>2</sub> Fin-Based Flash Synaptic Cells in AND Array Architecture for Binary Neural Networks. <i>IEEE Electron Device Letters</i> , 2022, 43, 142-145.	3.9	9
9	Neuron Circuits for Low-Power Spiking Neural Networks Using Time-To-First-Spike Encoding. <i>IEEE Access</i> , 2022, 10, 24444-24455.	4.2	8
10	Unsupervised Online Learning With Multiple Postsynaptic Neurons Based on Spike-Timing-Dependent Plasticity Using a Thin-Film Transistor-Type NOR Flash Memory Array. <i>Journal of Nanoscience and Nanotechnology</i> , 2019, 19, 6050-6054.	0.9	7
11	Hardware-Based Spiking Neural Network Using a TFT-Type AND Flash Memory Array Architecture Based on Direct Feedback Alignment. <i>IEEE Access</i> , 2021, 9, 73121-73132.	4.2	7
12	Spiking Neural Networks With Time-to-First-Spike Coding Using TFT-Type Synaptic Device Model. <i>IEEE Access</i> , 2021, 9, 78098-78107.	4.2	5
13	Initial synaptic weight distribution for fast learning speed and high recognition rate in STDP-based spiking neural network. <i>Solid-State Electronics</i> , 2020, 165, 107742.	1.4	4
14	On-chip trainable hardware-based deep Q-networks approximating a backpropagation algorithm. <i>Neural Computing and Applications</i> , 2021, 33, 9391-9402.	5.6	4
15	Review of candidate devices for neuromorphic applications. , 2019, , .		3
16	Grayscale Image Recognition Using Spike-Rate-Based Online Learning and Threshold Adjustment of Neurons in a Thin-Film Transistor-Type NOR Flash Memory Array. <i>Journal of Nanoscience and Nanotechnology</i> , 2019, 19, 6055-6060.	0.9	2
17	Variation-Tolerant Capacitive Array for Binarized Neural Network. <i>IEEE Electron Device Letters</i> , 2022, 43, 478-481.	3.9	2
18	Analog synaptic devices applied to spiking neural networks for reinforcement learning applications. <i>Semiconductor Science and Technology</i> , 2022, 37, 075002.	2.0	1