Abhinav

List of Publications by Year
in descending order

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Version: 2024-02-01

16	172	1307594 7	1199594 12
papers	citations	h-index	g-index

18	18	18	90
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Novel Approach to Model Threshold Voltage and Subthreshold Current of Graded-Doped Junctionless-Gate-All-Around (GD-JL-GAA) MOSFETs. Silicon, 2022, 14, 2989-2997.	3.3	11
2	Comparative Analysis & Study of Various Leakage Reduction Techniques for Short Channel Devices in Junctionless Transistors: A Review and Perspective. Silicon, 2022, 14, 4423-4445.	3.3	15
3	Modeling of Threshold Voltage and Subthreshold Current of Junctionless Channel-Modulated Dual-Material Double-Gate (JL-CM-DMDG) MOSFETs. Silicon, 2022, 14, 5495-5502.	3.3	3
4	A Novel Approach to Investigate the Impact of Hetero-High-K Gate Stack on SiGe Junctionless Gate-All-Around (JL-GAA) MOSFET. Silicon, 2022, 14, 1005-1012.	3.3	12
5	Keeper Effect on Nano Scale Silicon Domino Logic Transistors. Silicon, 2022, 14, 6769-6776.	3.3	4
6	A Novel Approach to Investigate Analog and Digital Circuit Applications of Silicon Junctionless-Double-Gate (JL-DG) MOSFETs. Silicon, 2022, 14, 7577-7584.	3.3	8
7	A Novel Technique to Investigate the Impact of Temperature and Process Parameters on Electrostatic and Analog/RF Performance of Channel Modulated Junctionless Gate-all-around (CM-JL-GAA) MOSFET. Silicon, 2022, 14, 10613-10622.	3.3	3
8	Temperature-Dependent Analytical Modeling of Graded-Channel Gate-All-Around (GC-GAA) Junctionless Field-Effect Transistors (JLFETs). Journal of Electronic Materials, 2021, 50, 3686-3691.	2.2	5
9	An Analysis of Si-tube Based Double-Material Double Gate-All-Around (DMDGAA) MOSFETs. , 2020, , .		5
10	Reduction of self-heating effect using selective buried oxide (SELBOX) charge plasma based junctionless transistor. AEU - International Journal of Electronics and Communications, 2018, 95, 162-169.	2.9	15
11	Potential Modeling of Oxide Engineered Doping-Less Dual-Material-Double-Gate Siâ€“Ge MOSFET and Its Application. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 1115-1122.	0.5	5
12	Analytical Modelling and Analysis of Spacer Induced Shallow Source/Drain Extension Junction-Less Double Gate (SDE-JLDG) MOSFET Incorporating Fringing Field Effects. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 168-177.	0.5	1
13	Reliability analysis of Junction-less Double Gate (JLDG) MOSFET for analog/RF circuits for high linearity applications. Microelectronics Journal, 2017, 64, 60-68.	2.0	30
14	Analytical model and performance investigation of electric potential for junctionless cylindrical surrounding gate (JLCSG) MOSFET. , 2017, , .		5
15	Analytical surface potential modeling and simulation of junction-less double gate (JLDG) MOSFET for ultra low-power analog/RF circuits. Microelectronics Journal, 2015, 46, 916-922.	2.0	45
16	Linearity Distortion & Thermal Stability Analysis of Negative Capacitance based Cylindrical Junction-less Transistors (NC-CyJLT). Silicon, 0, , 1.	3.3	1