

# Awais Mehmood Kamboh

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/5980183/publications.pdf>

Version: 2024-02-01

16  
papers

220  
citations

1307594

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h-index

1372567

10  
g-index

17  
all docs

17  
docs citations

17  
times ranked

242  
citing authors

#	ARTICLE	IF	CITATIONS
1	Dynamic Mode Decomposition Based Epileptic Seizure Detection from Scalp EEG. IEEE Access, 2018, 6, 38683-38692.	4.2	71
2	Mallat's Scattering Transform Based Anomaly Sensing for Detection of Seizures in Scalp EEG. IEEE Access, 2017, 5, 16919-16929.	4.2	27
3	Classification of multi-class motor imagery EEG using four band common spatial pattern. , 2017, 2017, 1034-1037.		16
4	A CMOS Micro-power and Area Efficient Neural Recording and Stimulation Front-End for Biomedical Applications. Circuits, Systems, and Signal Processing, 2015, 34, 1725-1746.	2.0	14
5	TrojanZero: Switching Activity-Aware Design of Undetectable Hardware Trojans with Zero Power and Area Footprint. , 2019, , .		14
6	Motion artifact reduction from PPG signals during intense exercise using filtered X-LMS. , 2017, , .		13
7	Epileptic Seizure Detection With a Reduced Montage: A Way Forward for Ambulatory EEG Devices. IEEE Access, 2020, 8, 65880-65890.	4.2	11
8	Comparison of Classifier Architectures for Online Neural Spike Sorting. IEEE Transactions on Neural Systems and Rehabilitation Engineering, 2017, 25, 334-344.	4.9	9
9	The NMT Scalp EEG Dataset: An Open-Source Annotated Dataset of Healthy and Pathological EEG Recordings for Predictive Modeling. Frontiers in Neuroscience, 2021, 15, 755817.	2.8	9
10	Low SNR neural spike detection using scaled energy operators for implantable brain circuits. , 2017, 2017, 1074-1077.		8
11	A robust approach towards epileptic seizure detection. , 2016, , .		7
12	Formal Verification of Gate-Level Multiple Side Channel Parameters to Detect Hardware Trojans. Communications in Computer and Information Science, 2017, , 75-92.	0.5	7
13	McSeVIC: A Model Checking Based Framework for Security Vulnerability Analysis of Integrated Circuits. IEEE Access, 2018, 6, 32240-32257.	4.2	7
14	Using gate-level side channel parameters for formally analyzing vulnerabilities in integrated circuits. Science of Computer Programming, 2019, 171, 42-66.	1.9	5
15	ForASec: Formal Analysis of Hardware Trojan-Based Security Vulnerabilities in Sequential Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1167-1180.	2.7	2
16	Power & throughput optimized lifting architecture for Wavelet Packet Transform. , 2014, , .		0