

Jes s L zaro

List of Publications by Year in descending order

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Version: 2024-02-01

86
papers

790
citations

687220

13
h-index

642610

23
g-index

88
all docs

88
docs citations

88
times ranked

890
citing authors

#	ARTICLE	IF	CITATIONS
1	Hardware implementation of optical flow constraint equation using FPGAs. Computer Vision and Image Understanding, 2005, 98, 462-490.	3.0	66
2	Cyber-security in substation automation systems. Renewable and Sustainable Energy Reviews, 2016, 54, 1552-1562.	8.2	55
3	Malguki: an RSSI based ad hoc location algorithm. Microprocessors and Microsystems, 2004, 28, 403-409.	1.8	53
4	Fault location on two-terminal transmission lines based on voltages. IET Generation, Transmission and Distribution, 1996, 143, 1.	1.1	49
5	Smart Sensor: SoC Architecture for the Industrial Internet of Things. IEEE Internet of Things Journal, 2019, 6, 6567-6577.	5.5	33
6	Implementation of a modified Fuzzy C-Means clustering algorithm for real-time applications. Microprocessors and Microsystems, 2005, 29, 375-380.	1.8	31
7	FPGA technology for multi-axis control systems. Mechatronics, 2009, 19, 258-268.	2.0	29
8	PRP and HSR for High Availability Networks in Power Utility Automation: A Method for Redundant Frames Discarding. IEEE Transactions on Smart Grid, 2015, 6, 2325-2332.	6.2	27
9	Neuro semantic thresholding using OCR software for high precision OCR applications. Image and Vision Computing, 2010, 28, 571-578.	2.7	22
10	Tornado: A self-reconfiguration control system for core-based multiprocessor CSoPCs. Journal of Systems Architecture, 2007, 53, 629-643.	2.5	19
11	On the Utilization of System-on-Chip Platforms to Achieve Nanosecond Synchronization Accuracies in Substation Automation Systems. IEEE Transactions on Smart Grid, 2017, 8, 1932-1942.	6.2	19
12	Cyber-Physical Production System Gateway Based on a Programmable SoC Platform. IEEE Access, 2017, 5, 20408-20417.	2.6	18
13	Security mechanisms to protect IEEE 1588 synchronization: State of the art and trends. , 2015, , .		16
14	A Survey on Vulnerabilities and Countermeasures in the Communications of the Smart Grid. Electronics (Switzerland), 2021, 10, 1881.	1.8	15
15	SOM Segmentation of gray scale images for optical recognition. Pattern Recognition Letters, 2006, 27, 1991-1997.	2.6	13
16	IEEE 1588 Transparent Clock architecture for FPGA-based network devices. , 2013, , .		13
17	Intelligent gateway for Industry 4.0-compliant production. , 2016, , .		13
18	SEU emulation in industrial SoCs combining microprocessor and FPGA. Reliability Engineering and System Safety, 2018, 170, 53-63.	5.1	13

#	ARTICLE	IF	CITATIONS
19	A Fixed-Latency Architecture to Secure GOOSE and Sampled Value Messages in Substation Systems. IEEE Access, 2021, 9, 51646-51658.	2.6	13
20	A top-down design for the train communication network. , 0, , .		12
21	Fast and accurate SEU-tolerance characterization method for Zynq SoCs. , 2014, , .		12
22	Estimating the SEU failure rate of designs implemented in FPGAs in presence of MCUs. Microelectronics Reliability, 2017, 78, 85-92.	0.9	12
23	Multiprocessor SoPC-Core for FAT volume computation. Microprocessors and Microsystems, 2005, 29, 421-434.	1.8	11
24	High availability automation networks: PRP and HSR ring implementations. , 2012, , .		11
25	Real-Time Stereo Vision Processing System in a FPGA. Industrial Electronics Society (IECON), Annual Conference of IEEE, 2006, , .	0.0	10
26	Hardware architecture for a general regression neural network coprocessor. Neurocomputing, 2007, 71, 78-87.	3.5	10
27	An automatic experimental set-up for robustness analysis of designs implemented on SRAM FPGAS. , 2011, , .		9
28	Robustness of different TMR granularities in shared wishbone architectures on SRAM FPGA. , 2012, , .		9
29	GPS-less location algorithm for wireless sensor networks. Computer Communications, 2007, 30, 2904-2916.	3.1	8
30	I2Csec: A secure serial Chip-to-Chip communication protocol. Journal of Systems Architecture, 2011, 57, 206-213.	2.5	8
31	FPGA implemented cut-through vs store-and-forward switches for reliable ethernet networks. , 2014, , .		8
32	CPPS Gateway - Implementation of Modbus and Profibus on a SoC programmable platform. IEEE Latin America Transactions, 2018, 16, 335-341.	1.2	8
33	Simulink/Modelsim Simulabel VHDL PID Core for Industrial SoPC Multiaxis Controllers. Industrial Electronics Society (IECON), Annual Conference of IEEE, 2006, , .	0.0	7
34	PRP and HSR version 1 (IEC 62439-3 Ed.2), improvements and a prototype implementation. , 2013, , .		7
35	FTL-CFree: A Fuzzy Real-Time Language for Runtime Verification. IEEE Transactions on Industrial Informatics, 2014, 10, 1670-1683.	7.2	7
36	An implementation of a general regression neural network on FPGA with direct Matlab link. , 0, , .		6

#	ARTICLE	IF	CITATIONS
37	Robustness Analysis of Different AES Implementations on SRAM Based FPGAs. , 2011, , .		6
38	Cost-effective redundancy for ethernet train communications using HSR. , 2014, , .		6
39	An Electronic Secure Voting System Based on Automatic Paper Ballot Reading. Lecture Notes in Computer Science, 2004, , 470-477.	1.0	5
40	MACsec Layer 2 Security in HSR Rings in Substation Automation Systems. Energies, 2017, 10, 162.	1.6	5
41	Secure Protocol and IP Core for Configuration of Networking Hardware IPs in the Smart Grid. Energies, 2018, 11, 510.	1.6	5
42	Evaluating Latency in Multiprocessing Embedded Systems for the Smart Grid. Energies, 2021, 14, 3322.	1.6	5
43	Multi-architectural 128 bit AES-CBC Core based on Open-Source Hardware AES Implementations for Secure Industrial Communications. , 2006, , .		4
44	A novel SoC architecture for a MVB slave node. , 2008, , .		4
45	Duplicate and circulating frames discard methods for PRP and HSR (IEC62439-3). , 2013, , .		4
46	Securing IEEE 1588 messages with message authentication codes based on the KECCAK cryptographic algorithm implemented in FPGAs. , 2014, , .		4
47	A novel BRAM content accessing and processing method based on FPGA configuration bitstream. Microprocessors and Microsystems, 2017, 49, 64-76.	1.8	4
48	System-on-Programmable-Chip AES-GCM implementation for wire-speed cryptography for SAS. , 2018, , .		4
49	A Self-Reconfiguration Framework for Multiprocessor CSoPCs. Lecture Notes in Computer Science, 2004, , 1124-1126.	1.0	4
50	AES-Galois Counter Mode Encryption/Decryption FPGA Core for Industrial and Residential Gigabit Ethernet Communications. Lecture Notes in Computer Science, 2009, , 312-317.	1.0	4
51	Analysing the interference of Xen hypervisor in the network speed. , 2020, , .		4
52	Modified Fuzzy C-Means Clustering Algorithm for Real-Time Applications. Lecture Notes in Computer Science, 2003, , 1087-1090.	1.0	3
53	Location algorithm for wireless sensor networks in industrial applications. , 0, , .		3
54	OSCRYB: Open Source CRYpto-Bridge for Secure Ethernet point-to-point Industrial Communications. , 2007, , .		3

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55	Decompression dual core for SoPC applications in high speed FPGA. , 2007, , .		3
56	SoPC Implementation of the TP-KNX Protocol for Domotic Applications. , 2008, , .		3
57	Known-blocking. Synchronization method for reliable processor using TMR & DPR in SRAM FPGAs. , 2011, , .		3
58	Nanosecond accuracy using SoC platforms. , 2014, , .		3
59	Dependability in FPGAs, a Review. , 2015, , .		3
60	High Throughput Serpent Encryption Implementation. Lecture Notes in Computer Science, 2004, , 996-1000.	1.0	2
61	Node Synchronization in Wireless Sensor Networks. , 2006, , .		2
62	PCIREX: A Fast Prototyping Platform for TMR Dynamically Reconfigurable Systems. , 2009, , .		2
63	1588-aware High-Availability Cyber-Physical Production Systems. , 2015, , .		2
64	Synchronizing NTP Referenced SCADA Systems Interconnected by High-availability Networks. , 2020, , .		2
65	Secure Critical Traffic of the Electric Sector over Time-Sensitive Networking. , 2020, , .		2
66	Fast and efficient address search in System-on-a-Programmable-Chip using binary trees. Computers and Electrical Engineering, 2021, 96, 107403.	3.0	2
67	High-Performance Computing Architecture for Sample Value Processing in the Smart Grid. IEEE Access, 2022, 10, 12208-12218.	2.6	2
68	Time Sensitive Networking Protocol Implementation for Linux End Equipment. Technologies, 2022, 10, 55.	3.0	2
69	Run-Time Reconfigurable Hardware-Software Architecture for PID Motor Control IP Cores. , 2006, , .		1
70	Configurable-System-on-Programmable-Chip for Power Electronics Control Applications. , 2008, , .		1
71	DNAX-BCU: An Un-clonable Cost-conscious SoPC Implementation for Bus Coupling Units of the European Installation Bus. , 2009, , .		1
72	SafeSoC: A fault-tolerant-by-redundancy evaluation card for high speed serial communications. , 2016, , .		1

#	ARTICLE	IF	CITATIONS
73	Fast and efficient FPGA prototype system for embedded control algorithms in electric traction. , 2019, , .		1
74	Secure Ethernet Point-to-Point Links for Autonomous Electronic Ballot Boxes. Lecture Notes in Computer Science, 2008, , 603-614.	1.0	1
75	An Autonomous Fault Tolerant System for CAN Communications. Lecture Notes in Computer Science, 2010, , 281-290.	1.0	1
76	Embedded firewall for on-chip bus transactions. Computers and Electrical Engineering, 2022, 98, 107707.	3.0	1
77	Test workbench for electronic telecommunication systems. , 0, , .		0
78	Architecture of a Real-Time Wavelet Transform Calculation SoPC Core for Industrial Applications. Industrial Electronics Society (IECON), Annual Conference of IEEE, 2006, , .	0.0	0
79	High-precision DRM Demodulator for Remote Monitoring. , 2007, , .		0
80	The Train Communication Network: Standardization goes aboard. , 2010, , .		0
81	NoCmodel: An extensible framework for Network-on-Chips modeling. , 2011, , .		0
82	SDR control interface: An FPGA based infrastructure for control of VPX Software Defined Radio systems. , 2013, , .		0
83	Memory requirements analysis for PRP and HSR hardware implementations on FPGAs. , 2013, , .		0
84	System-on-Chip implementation of Reliable Ethernet Networks nodes. , 2013, , .		0
85	Electronic control board for student Rocket. , 2020, , .		0
86	Specific Electronic Platform to Test the Influence of Hypervisors on the Performance of Embedded Systems. Technologies, 2022, 10, 65.	3.0	0