Muhammad Nadzir Marsono

List of Publications by Year
in descending order

105	693	686830 13	752256 20
papers	citations	h-index	g-index

105	105	105	610
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	RtFog: A Real-Time FPGA-Based Fog Node With Remote Dynamically Reconfigurable Application Plane for Fog Analytics Redeployment. IEEE Transactions on Green Communications and Networking, 2022, 6, 341-351.	3.5	3
2	PEW: Prediction-Based Early Dark Cores Wake-up Using Online Ridge Regression for Many-Core Systems. IEEE Access, 2021, 9, 124087-124099.	2.6	3
3	Collaborative detection and mitigation of DDoS in software-defined networks. Journal of Supercomputing, 2021, 77, 13166-13190.	2.4	13
4	A Centralized Token-based Medium Access Control Mechanism for Wireless Network-on-Chip. , 2021, , .		2
5	Early Flow Table Eviction Impact on Delay and Throughput in Software-Defined Networks. , 2021, , .		4
6	An FPGA-based Middlebox with Remote Dynamically Reconfigurable Application Plane. , 2021, , .		0
7	DTaPO: Dynamic Thermal-Aware Performance Optimization for Dark Silicon Many-Core Systems. Electronics (Switzerland), 2020, 9, 1980.	1.8	6
8	Edge Computing Intelligence Using Robust Feature Selection for Network Traffic Classification in Internet-of-Things. IEEE Access, 2020, 8, 224059-224070.	2.6	13
9	Flow-Aware Elephant Flow Detection for Software-Defined Networks. IEEE Access, 2020, 8, 72585-72597.	2.6	36
10	Collaborative Detection and Mitigation of Distributed Denial-of-Service Attacks on Software-Defined Network. Mobile Networks and Applications, 2020, 25, 1338-1347.	2.2	14
11	Impact of Early Estimation of Statistical Flow Features in On-line P2P Classification. , 2020, , .		0
12	Interleaved Incremental/Decremental Support Vector Machine for Embedded System. , 2019, , .		0
13	Temperature-Aware Task Scheduling for Dark Silicon Many-Core System-on-Chip. , 2019, , .		5
14	A streaming multi-class support vector machine classification architecture for embedded systems. Indonesian Journal of Electrical Engineering and Computer Science, 2019, 16, 1286.	0.7	0
15	Improved quantum circuit modelling based on Heisenberg representation. Quantum Information Processing, 2018, 17, 1.	1.0	2
16	A linked list run-length-based single-pass connected component analysis for real-time embedded hardware. Journal of Real-Time Image Processing, 2018, 15, 197-215.	2.2	21
17	Rapid Prototyping of NoC-based MPSoC Based on Dataflow Modeling of Real-World Applications. , 2018, , .		1
18	First Line Defense Against Spreading New Malware in the Network. , 2018, , .		1

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19	An FPGA-based quantum circuit emulation framework using heisenberg representation. International Journal of Quantum Information, 2018, 16, 1850052.	0.6	0
20	drDRM: A PUF-Based Dynamically Reconfigurable DRM Mechanism for FPGA-Based Platform. , 2018, , .		0
21	Impact of Packet Inter-arrival Time Features for Online Peer-to-Peer (P2P) Classification. International Journal of Electrical and Computer Engineering, 2018, 8, 2521.	0.5	3
22	Performance Evaluation of Centralized Reconfigurable Transmitting Power Scheme in Wireless Network-on-chip. Telkomnika (Telecommunication Computing Electronics and Control), 2018, 16, 2844.	0.6	1
23	Cooperative Learning for Distributed In-Network Traffic Classification. IOP Conference Series: Materials Science and Engineering, 2017, 190, 012010.	0.3	0
24	Ping-lock round robin arbiter. Microelectronics Journal, 2017, 63, 81-93.	1.1	9
25	Hardware transactional memory architecture with adaptive version management for multi-processor FPGA platforms. Journal of Systems Architecture, 2017, 73, 42-52.	2.5	3
26	Adaptive Packet Relocator in Wireless Network-on-Chip (WiNoC). Communications in Computer and Information Science, 2017, , 719-735.	0.4	2
27	hpFog: A FPGA-Based Fog Computing Platform. , 2017, , .		6
28	ProNoC: A low latency network-on-chip based many-core system-on-chip prototyping platform. Microprocessors and Microsystems, 2017, 54, 60-74.	1.8	47
29	Reconfigurable logic embedded architecture of support vector machine linear kernel. , 2017, , .		2
30	Incremental high throughput network traffic classifier. , 2017, , .		0
31	Multi-stage Feature Selection for On-Line Flow Peer-to-Peer Traffic Identification. Communications in Computer and Information Science, 2017, , 509-523.	0.4	3
32	A Customized Reconfiguration Controller with Remote Direct ICAP Access for Dynamically Reconfigurable Platform. Telkomnika (Telecommunication Computing Electronics and Control), 2017, 15, 570.	0.6	0
33	ONLINE PEER-TO-PEER TRAFFIC IDENTIFICATION BASED ON COMPLEX EVENTS PROCESSING OF TRAFFIC EVENT SIGNATURES. Jurnal Teknologi (Sciences and Engineering), 2016, 78, .	0.3	1
34	Online Incremental Learning for High Bandwidth Network Traffic Classification. Applied Computational Intelligence and Soft Computing, 2016, 2016, 1-13.	1.6	10
35	FPGA-Based Real-Time Moving Target Detection System for Unmanned Aerial Vehicle Application. International Journal of Reconfigurable Computing, 2016, 2016, 1-16.	0.2	19
36	An FPGA-Based Quantum Computing Emulation Framework Based on Serial-Parallel Architecture. International Journal of Reconfigurable Computing, 2016, 2016, 1-18.	0.2	26

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37	Low latency network-on-chip router using static straight allocator. , 2016, , .		6
38	Improved Flow Control for Minimal Fully Adaptive Routing in 2D Mesh NoC. , 2016, , .		4
39	Online network traffic classification with incremental learning. Evolving Systems, 2016, 7, 129-143.	2.4	11
40	A modular architecture for dynamically reconfigurable middlebox with customized reconfiguration handler. , 2016, , .		1
41	rrBox: A remote dynamically reconfigurable network processing middlebox. , 2015, , .		2
42	A Closed Loop Transmitting Power Self-Calibration Scheme for Energy Efficient WiNoC Architectures. , 2015, , .		4
43	Online data stream classification with incremental semi-supervised learning. , 2015, , .		8
44	Cooperative learning for online in-network performance monitoring. , 2015, , .		1
45	Incorporating known malware signatures to classify new malware variants in network traffic. International Journal of Network Management, 2015, 25, 471-489.	1.4	11
46	FEATURE SELECTION AND MACHINE LEARNING CLASSIFICATION FOR MALWARE DETECTION. Jurnal Teknologi (Sciences and Engineering), 2015, 77, .	0.3	26
47	Low Latency Network-on-Chip Router Microarchitecture Using Request Masking Technique. International Journal of Reconfigurable Computing, 2015, 2015, 1-13.	0.2	21
48	Hardware/software partitioning of embedded System-on-Chip applications. , 2015, , .		9
49	Adaptive Configurable Transactional Memory for Multi-processor FPGA Platforms. , 2015, , .		1
50	Built-in Self Test Power and Test Time Analysis in On-chip Networks. Circuits, Systems, and Signal Processing, 2015, 34, 1057-1075.	1.2	2
51	Virtual Channel and Switch Allocation for Low Latency Network-on-Chip Routers. , 2015, , .		2
52	Automated Dataset Generation for Training Peer-to-Peer Machine Learning Classifiers. Journal of Network and Systems Management, 2015, 23, 89-110.	3.3	4
53	2-D DWT System Architecture for Image Compression. Journal of Signal Processing Systems, 2015, 78, 131-137.	1.4	9
54	A CLOSED LOOP POWER MANAGER FOR TRANSMISSION POWER CONTROL IN WIRELESS NETWORK-ON-CHIP ARCHITECTURES. Jurnal Teknologi (Sciences and Engineering), 2015, 75, .	0.3	0

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55	Network Partitioning Domain Knowledge Multiobjective Application Mapping for Large-Scale Network-on-Chip. Applied Computational Intelligence and Soft Computing, 2014, 2014, 1-10.	1.6	2
56	Hardware transactional memory on multi-processor FPGA platform. , 2014, , .		1
57	Packet logging mechanism for adaptive online fault detection on Network-on-Chip. , 2014, , .		2
58	A Closed Loop Control based Power Manager for WiNoC Architectures. , 2014, , .		2
59	FPGA-based quantum circuit emulation: A case study on Quantum Fourier transform. , 2014, , .		3
60	rrBox: A Remote Dynamically Reconfigurable Middlebox for Network Protection. , 2014, , .		1
61	Remote dynamically reconfigurable platform using NetFPGA. , 2014, , .		0
62	Partially adaptive look-ahead routing for low latency Network-on-Chip. , 2014, , .		5
63	Optimization of structure and system latency in evolvable block-based neural networks using genetic algorithm. Neurocomputing, 2014, 145, 285-302.	3.5	12
64	Hardware implementation of evolvable block-based neural networks utilizing a cost efficient sigmoid-like activation function. Neurocomputing, 2014, 140, 228-241.	3.5	16
65	Malware detection using augmented naive Bayes with domain knowledge and under presence of class noise. International Journal of Information and Computer Security, 2014, 6, 179.	0.2	1
66	Stateless Malware Packet Detection by Incorporating Naive Bayes with Known Malware Signatures. Applied Computational Intelligence and Soft Computing, 2014, 2014, 1-8.	1.6	14
67	rrBox: Remote dynamically reconfigurable middlebox using NetFPGA. , 2014, , .		1
68	Selection of On-line Features for Peer-to-Peer Network Traffic Classification. Advances in Intelligent Systems and Computing, 2014, , 379-390.	0.5	8
69	Online Data Stream Learning and Classification with Limited Labels. Proceeding of the Electrical Engineering Computer Science and Informatics, 2014, 1, .	0.0	2
70	Analysis of features selection for P2P traffic detection using support vector machine. , 2013, , .		4
71	Network partitioning and GA heuristic crossover for NoC application mapping. , 2013, , .		4
72	Online NetFPGA decision tree statistical traffic classifier. Computer Communications, 2013, 36, 1329-1340.	3.1	25

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73	HW/SW co-design of reconfigurable hardware-based genetic algorithm in FPGAs applicable to a variety of problems. Computing (Vienna/New York), 2013, 95, 863-896.	3.2	11
74	Biometric encryption based on a fuzzy vault scheme with a fast chaff generation algorithm. Future Generation Computer Systems, 2013, 29, 800-810.	4.9	33
75	Co-simulation methodology for improved design and verification of hardware neural networks. , 2013, , .		3
76	Feasible transition path generation for EFSM-based system testing. , 2013, , .		4
77	Retraining Mechanism for On-Line Peer-to-Peer Traffic Classification. Advances in Intelligent Systems and Computing, 2013, , 373-382.	0.5	4
78	A Semi-Analytical Approach to Study the Energy Consumption of On-Chip Networks Testing. Journal of Low Power Electronics, 2013, 9, 189-197.	0.6	2
79	Parameterizable Decision Tree Classifier on NetFPGA. Advances in Intelligent Systems and Computing, 2013, , 119-128.	0.5	3
80	Evolvable Block-based Neural Networks for real-time classification of heart arrhythmia From ECG signals. , 2012, , .		6
81	s.RABILA2: An optimal VLSI routing algorithm with buffer insertion using iterative RLC model. , 2012, , .		1
82	Evolvable Block-based Neural Networks for classification of driver drowsiness based on heart rate variability. , 2012, , .		10
83	GA-based parameter tuning in finger-vein biometric embedded systems for information security. , 2012, , .		6
84	Second-stage tuning procedure for analogue CMOS design reuse methodology. Electronics Letters, 2012, 48, 990-992.	0.5	2
85	A Hardware/Software Co-design Architecture of Canny Edge Detection. , 2012, , .		2
86	A hybrid heuristics-statistical peer-to-peer traffic classifier. , 2012, , .		1
87	Packet-level open-digest fingerprinting for spam detection on middleboxes. International Journal of Network Management, 2012, 22, 12-26.	1.4	6
88	A Network-on-Chip simulation framework for homogeneous Multi-Processor System-on-Chip. , 2011, , .		0
89	Multi-TAP architecture for IP core testing and debugging on network-on-chip. , 2011, , .		1
90	Network Worm Propagation Model Based on a Campus Network Topology. , 2011, , .		2

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91	An FPGA hardware architecture of Nilsimsa fingerprinting algorithm. , 2011, , .		0
92	A framework for automated malcode signatures generation. , 2010, , .		1
93	A hardware architecture of Prewitt edge detection. , 2010, , .		22
94	Detecting Worms Using Data Mining Techniques: Learning in the Presence of Class Noise. , 2010, , .		7
95	A three-class heuristics technique: Generating training corpus for Peer-to-Peer traffic classification. , 2010, , .		4
96	Hardware Acceleration of OpenSSL Cryptographic Functions for High-Performance Internet Security. , 2010, , .		18
97	CODESL: A Framework for System-Level Modelling, Co-simulation and Design-Space Exploration of Embedded Systems Based on System-on-Chip. , 2010, , .		1
98	Embedded vision systems for ship recognition. , 2009, , .		5
99	A spam rejection scheme during SMTP sessions based on layer-3 e-mail classification. Journal of Network and Computer Applications, 2009, 32, 236-257.	5.8	7
100	Targeting spam control on middleboxes: Spam detection based on layer-3 e-mail content classification. Computer Networks, 2009, 53, 835-848.	3.2	18
101	Prioritized eâ€mail servicing to reduce nonâ€spam delay and loss: A performance analysis. International Journal of Network Management, 2008, 18, 325-344.	1.4	5
102	Binary LNS-based naiÌˆve Bayes inference engine for spam control: noise analysis and FPGA implementation. IET Computers and Digital Techniques, 2008, 2, 56.	0.9	18
103	Performance Analysis of Server-Side Spam Control Strategies Based on Layer-3 Classification. , 2007, , .		2
104	Rejecting Spam during SMTP Sessions. , 2007, , .		1
105	Distributed Layer-3 E-Mail Classification for Spam Control. , 2006, , .		6