Kailash Chandra Ray

List of Publications by Year
in descending order

38 papers	770 citations	687363 13 h-index	610901 24 g-index
38 all docs	38 docs citations	38 times ranked	674 citing authors

#	Article	IF	Citations
1	An Efficient Method for Detection and Localization of Myocardial Infarction. IEEE Transactions on Instrumentation and Measurement, 2022, 71, 1-12.	4.7	11
2	A Low-Overhead Reconfigurable RISC-V Quad-Core Processor Architecture for Fault-Tolerant Applications. IEEE Access, 2022, 10, 44136-44146.	4.2	6
3	ASIC Implementation of Low PAPR Multidevice Variable-Rate Architecture for IEEE 802.11ah. IEEE Transactions on Instrumentation and Measurement, 2021, 70, 1-10.	4.7	1
4	Multiuser Variable Rate GO-OFDMA Architecture and Its FPGA Prototype. IEEE Systems Journal, 2020, 14, 2455-2463.	4.6	1
5	A Coupled Variable Input LCG Method and its VLSI Architecture for Pseudorandom Bit Generation. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 1011-1019.	4.7	24
6	High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3944-3953.	5.4	16
7	Performance Analysis and FPGA Prototype of Variable Rate GO-OFDMA Baseband Transmission Scheme. Wireless Personal Communications, 2019, 108, 785-809.	2.7	4
8	Design and ASIC Implementation of a Reconfigurable Fault-Tolerant ALU for Space Applications. , 2019, , .		5
9	A Basis Function for DCT Based Discrete Orthogonal S-Transform. , 2019, , .		0
10	Area-Efficient Parallel-Prefix Binary Comparator. , 2019, , .		1
11	An Efficient Signal Processing Technique for Automated Myocardial Infarction Detection. , 2019, , .		0
12	Modified Dual-CLCG Method and its VLSI Architecture for Pseudorandom Bit Generation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 989-1002.	5.4	27
13	CORDIC-Based VLSI Architectures of Running DFT with Refreshing Mechanism. Journal of Signal Processing Systems, 2019, 91, 539-550.	2.1	3
14	FPGA Prototype and Real Time Analysis of Multiuser Variable Rate CI-GO-OFDMA. IEEE Transactions on Instrumentation and Measurement, 2018, 67, 538-546.	4.7	7
15	Sparse representation of ECG signals for automated recognition of cardiac arrhythmias. Expert Systems With Applications, 2018, 105, 49-64.	7.6	100
16	An Efficient VLSI Architecture for Computation of Discrete Fractional Fourier Transform. Journal of Signal Processing Systems, 2018, 90, 1569-1580.	2.1	3
17	Secure OFDM based on Coupled Linear Congruential Generator and its FPGA Prototype. , 2018, , .		0
18	Design and FPGA Prototype of 1024- bit Blum-Blum-Shub PRBG Architecture. , 2018, , .		8

#	Article	IF	Citations
19	A Personalized Point-of-Care Platform for Real-Time ECG Monitoring. IEEE Transactions on Consumer Electronics, 2018, 64, 452-460.	3.6	23
20	Automated recognition of cardiac arrhythmias using sparse decomposition over composite dictionary. Computer Methods and Programs in Biomedicine, 2018, 165, 175-186.	4.7	20
21	Development of robust, fast and efficient QRS complex detector: a methodological review. Australasian Physical and Engineering Sciences in Medicine, 2018, 41, 581-600.	1.3	28
22	A Personalized Arrhythmia Monitoring Platform. Scientific Reports, 2018, 8, 11395.	3.3	24
23	ECG Signal Analysis Using DCT-Based DOST and PSO Optimized SVM. IEEE Transactions on Instrumentation and Measurement, 2017, 66, 470-478.	4.7	183
24	Application of variational mode decomposition and ABC optimized DAG-SVM in arrhythmia analysis. , 2017, , .		5
25	CORDIC-based parallel architecture for one dimensional discrete Mellin transform. , 2016, , .		1
26	Efficient methodology for electrocardiogram beat classification. IET Signal Processing, 2016, 10, 825-832.	1.5	28
27	Cardiac arrhythmia beat classification using DOST and PSO tuned SVM. Computer Methods and Programs in Biomedicine, 2016, 136, 163-177.	4.7	87
28	Low-complexity CORDIC-based VLSI design and FPGA prototype of CI-OFDMA system for next-generation. , 2016, , .		2
29	CORDIC-based VLSI architecture for implementing CI-OFDM and its FPGA prototype. , 2016, , .		0
30	A comparative study of multivariate approach with neural networks and support vector machines for arrhythmia classification. , 2015, , .		11
31	Nonâ€singular sequence foldingâ€based pseudorandom key generation algorithm for cryptographic processor. Security and Communication Networks, 2015, 8, 4019-4027.	1.5	2
32	FPGA Prototype of Low Latency BBS PRNG. , 2015, , .		11
33	A knowledge-based real time embedded platform for arrhythmia beat classification. Biomedical Engineering Letters, 2015, 5, 271-280.	4.1	25
34	ARM-based arrhythmia beat monitoring system. Microprocessors and Microsystems, 2015, 39, 504-511.	2.8	39
35	FPGA implementation of stream cipher using Toeplitz Hash function. , 2014, , .		7
36	Low Latency Hybrid CORDIC Algorithm. IEEE Transactions on Computers, 2014, 63, 3066-3078.	3.4	46

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37	Hardware efficient design of Variable Length FFT Processor. , 2011, , .		5
38	High Throughput VLSI Architecture for Blackman Windowing in Real Time Spectral Analysis. Journal of Computers, 2008, 3, .	0.4	6