

# Gaurav Kaushal

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/5878565/publications.pdf>

Version: 2024-02-01

21  
papers

214  
citations

1040056

9  
h-index

996975

15  
g-index

21  
all docs

21  
docs citations

21  
times ranked

169  
citing authors

#	ARTICLE	IF	CITATIONS
1	Vertical Silicon Nanowire Gate-All-Around Field Effect Transistor Based Nanoscale CMOS. IEEE Electron Device Letters, 2011, 32, 1011-1013.	3.9	38
2	Vertical Nanowire CMOS Parasitic Modeling and its Performance Analysis. IEEE Transactions on Electron Devices, 2013, 60, 2943-2950.	3.0	25
3	A Degradation Model of Double Gate and Gate-All-Around MOSFETs With Interface Trapped Charges Including Effects of Channel Mobile Charge Carriers. IEEE Transactions on Device and Materials Reliability, 2014, 14, 689-697.	2.0	23
4	Radiation Effects in Si-NW GAA FET and CMOS Inverter: A TCAD Simulation Study. IEEE Transactions on Electron Devices, 2012, 59, 1563-1566.	3.0	22
5	Double Node Upset Tolerant RHBD15T SRAM Cell Design for Space Applications. IEEE Transactions on Device and Materials Reliability, 2020, 20, 181-190.	2.0	20
6	Electron transport in C3N monolayer: DFT analysis of volatile organic compound sensing. Chemical Physics Letters, 2021, 762, 138121.	2.6	18
7	Single-Event Multiple Effect Tolerant RHBD14T SRAM Cell Design for Space Applications. IEEE Transactions on Device and Materials Reliability, 2021, 21, 48-56.	2.0	17
8	Impact of series resistance on Si nanowire MOSFET performance. Journal of Computational Electronics, 2013, 12, 306-315.	2.5	13
9	Edge Engineered Graphene Nanoribbons as Nanoscale Interconnect: DFT Analysis. IEEE Nanotechnology Magazine, 2022, 21, 43-51.	2.0	10
10	Low power SRAM design for 14nm GAA Si-nanowire technology. Microelectronics Journal, 2015, 46, 1239-1247.	2.0	9
11	Device Circuit Co-Design Issues in Vertical Nanowire CMOS Platform. IEEE Electron Device Letters, 2012, 33, 934-936.	3.9	7
12	Tuning Source/Drain Extension Profile for Current Matching in Nanowire CMOS Logic. IEEE Nanotechnology Magazine, 2012, 11, 1033-1039.	2.0	3
13	A low power low noise analog front-end for ECG recording. Analog Integrated Circuits and Signal Processing, 2021, 109, 449-458.	1.4	3
14	Analytical model for quasi-ballistic transport in MOSFET including carrier backscattering. Journal of Computational Electronics, 2021, 20, 838-847.	2.5	2
15	Bandgap engineering in Ga and P doped armchair graphene nanoribbons: DFT analysis. Materials Today: Proceedings, 2022, 48, 647-649.	1.8	2
16	Electron transport in boron functionalised armchair graphene nanoribbons: Potential interconnects. Solid State Communications, 2021, 327, 114209.	1.9	1
17	Modeling of interface trap charges induced degradation in underlap DG and GAA MOSFETs. Microelectronics Reliability, 2021, 125, 114344.	1.7	1
18	A Robust SRAM cell for high performance Register File. , 2018, , .		0

#	ARTICLE	IF	CITATIONS
19	Soft Error-Resilient RHBD16T SRAM Cell in 32nm Technology. Advances in Computer and Electrical Engineering Book Series, 2021, , 171-188.	0.3	0
20	Understanding Electron Transport in oxygen decorated Zigzag Graphene nanoribbons for nanoscale interconnects. , 2021, , .		0
21	Enhanced metallicity in defected Zigzag graphene nanoribbons: Role of oxygen doping. MRS Advances, 2021, 6, 723-728.	0.9	0