Shanshan Liu

List of Publications by Year
in descending order

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Version: 2024-02-01

34	239	1040056	1058476
papers	citations	9	14
		h-index	g-index

34	34	34	158
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Tolerance of Siamese Networks (SNs) to Memory Errors: Analysis and Design. IEEE Transactions on Computers, 2023, 72, 1136-1149.	3.4	2
2	Selective Neuron Re-Computation (SNRC) for Error-Tolerant Neural Networks. IEEE Transactions on Computers, 2022, 71, 684-695.	3.4	3
3	Computing the Similarity Estimate Using Approximate Memory. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 1593-1604.	4.6	1
4	Error-Tolerant Data Sketches Using Approximate Nanoscale Memories and Voltage Scaling. IEEE Nanotechnology Magazine, 2022, 21, 16-22.	2.0	5
5	Probabilistic Approximate Computing at Nanoscales: From data structures to memories. IEEE Nanotechnology Magazine, 2022, 16, 16-24.	1.3	3
6	A Delta Sigma Modulator-Based Stochastic Divider. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3272-3283.	5.4	2
7	A Near-Sensor ECG Delineation and Arrhythmia Classification System. IEEE Sensors Journal, 2022, 22, 14217-14227.	4.7	4
8	Attacking Adaptive Cuckoo Filters: Too Much Adaptation Can Kill You. IEEE Transactions on Network and Service Management, 2022, 19, 5224-5236.	4.9	0
9	Editorial Special Issue on Circuits and Systems for Emerging Computing Paradigms. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2653-2654.	5.4	0
10	Detection of Limited Magnitude Errors in Emerging Multilevel Cell Memories by One-Bit Parity (OBP) or Two-Bit Parity (TBP). IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1792-1802.	4.6	14
11	Reduced Precision Redundancy for Reliable Processing of Data. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1960-1971.	4.6	6
12	Voting Margin: A Scheme for Error-Tolerant k Nearest Neighbors Classifiers for Machine Learning. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 2089-2098.	4.6	7
13	Protection of Associative Memories Using Combined Tag and Data Parity (CTDP). IEEE Nanotechnology Magazine, 2021, 20, 1-9.	2.0	4
14	Less-is-Better Protection (LBP) for memory errors in kNNs classifiers. Future Generation Computer Systems, 2021, 117, 401-411.	7.5	1
15	Remove Minimum (RM): An Error-Tolerant Scheme for Cardinality Estimate by HyperLogLog. IEEE Transactions on Dependable and Secure Computing, 2021, , 1-1.	5.4	1
16	Stochastic Dividers for Low Latency Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4102-4115.	5.4	10
17	High-Performance CMOS Latch Designs for Recovering All Single and Double Node Upsets. IEEE Transactions on Aerospace and Electronic Systems, 2021, 57, 4401-4415.	4.7	10
18	Exploiting Asymmetry in eDRAM Errors for Redundancy-Free Error-Tolerant Design. IEEE Transactions on Emerging Topics in Computing, 2020, , 1-1.	4.6	4

#	Article	IF	Citations
19	Result-Based Re-computation for Error-Tolerant Classification by a Support Vector Machine. IEEE Transactions on Artificial Intelligence, 2020, 1, 62-73.	4.7	15
20	Error-Tolerant Computation for Voting Classifiers With Multiple Classes. IEEE Transactions on Vehicular Technology, 2020, 69, 13718-13727.	6.3	7
21	Codes for Limited Magnitude Error Correction in Multilevel Cell Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1615-1626.	5.4	5
22	Scheme for periodical concurrent fault detection in parallel CRC circuits. IET Computers and Digital Techniques, 2020, 14, 80-85.	1.2	2
23	Design and Evaluation of Low-Complexity Radiation Hardened CMOS Latch for Double-Node Upset Tolerance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1925-1935.	5.4	28
24	A Layout-Based Soft Error Vulnerability Estimation Approach for Combinational Circuits Considering Single Event Multiple Transients (SEMTs). IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1109-1122.	2.7	17
25	A CMOS Majority Logic Gate and its Application to One-Step ML Decodable Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2620-2628.	3.1	3
26	Fault tolerant encoders for Single Error Correction and Double Adjacent Error Correction codes. Microelectronics Reliability, 2018, 81, 167-173.	1.7	6
27	A Double Error Correction Code for 32-Bit Data Words With Efficent Decoding. IEEE Transactions on Device and Materials Reliability, 2018, 18, 125-127.	2.0	10
28	Reducing the Power Consumption of Fault Tolerant Registers Through Hybrid Protection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1293-1302.	5.4	4
29	Comments on â€œExtend orthogonal Latin square codes for 32-bit data protection in memory applicationsâ€•Microelectron. Reliab. 63, 278â€“283 (2016). Microelectronics Reliability, 2017, 69, 126-129.	1.7	1
30	Single Event Transient Tolerant Bloom Filter Implementations. IEEE Transactions on Computers, 2017, 66, 1831-1836.	3.4	11
31	A method to recover critical bits under a double error in SEC-DED protected memories. Microelectronics Reliability, 2017, 73, 92-96.	1.7	5
32	Evaluating Direct Compare for Double Error-Correction Codes. IEEE Transactions on Device and Materials Reliability, 2017, 17, 802-804.	2.0	7
33	Extend orthogonal Latin square codes for 32-bit data protection in memory applications. Microelectronics Reliability, 2016, 63, 278-283.	1.7	13
34	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1603-1606.	3.1	28