Zhongfeng Wang

List of Publications by Year in Descending Order

117 papers	728 citations	15 h-index	20 g-index
174 ext. papers	1,142 ext. citations	3.2 avg, IF	4.99 L-index

#	Paper	IF	Citations
117	A Reliability Profile Based Low-Complexity Dynamic Schedule LDPC Decoding. *IEEE Access*, **2022**, 10, 3390-3399	3.5	
116	ETA: An Efficient Training Accelerator for DNNs Based on Hardware-Algorithm Co-Optimization.. *IEEE Transactions on Neural Networks and Learning Systems*, **2022**, PP,	10.3	1
115	LDPC decoding with locally informed dynamic scheduling based on the law of large numbers. *IET Communications*, **2022**, 16, 634-648	1.3	
114	An Efficient High-Throughput Structured-Light Depth Engine. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2022**, 1-12	2.6	0
113	THETA: A High-Efficiency Training Accelerator for DNNs With Triple-Side Sparsity Exploration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2022**, 1-13	2.6	0
112	Hybrid Stochastic-Binary Computing for Low-Latency and High-Precision Inference of CNNs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2022**, 1-14	3.9	0
111	An Efficient Reconfigurable Encoder for the IEEE 1901 Standard. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2022**, 1-5	2.6	
110	Piecewise Parabolic Approximate Computation Based on an Error-Flattened Segmenter and a Novel Quantizer. *Electronics (Switzerland)*, **2021**, 10, 2704	2.6	0
109	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-14	3.9	2
108	A Flexible and Efficient FPGA Accelerator for Various Large-Scale and Lightweight CNNs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-14	3.9	3
107	High-Throughput LDPC-CC Decoders Based on Storage, Arithmetic, and Control Improvements. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	
106	RVDFI: A RISC-V Architecture with Security Enforcement by High Performance Complete Data-Flow Integrity. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	
105	Memory-Efficient CNN Accelerator Based on Interlayer Feature Map Compression. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 1-14	3.9	2
104	An Improved Reliability-Based Decoding Algorithm for NB-LDPC Codes. *IEEE Communications Letters*, **2021**, 25, 1153-1157	3.8	2
103	High-Speed and Scalable FPGA Implementation of the Key Generation for the Leighton-Micali Signature Protocol **2021**,		3
102	Elbert: Fast Albert with Confidence-Window Based Early Exit **2021**,		1
101	A Hidden DCT-Based Invisible Watermarking Method for Low-Cost Hardware Implementations. *Electronics (Switzerland)*, **2021**, 10, 1465	2.6	1

100	An Efficient and Flexible Accelerator Design for Sparse Convolutional Neural Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 2936-2949	3.9	6
99	Low-Latency Hardware Accelerator for Improved Engle-Granger Cointegration in Pairs Trading. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 2911-2924	3.9	3
98	Counter Random Gradient Descent Bit-Flipping Decoder for LDPC Codes **2021**,		2
97	Evaluations on Deep Neural Networks Training Using Posit Number System. *IEEE Transactions on Computers*, **2021**, 70, 174-187	2.5	14
96	Design of High-Performance and Area-Efficient Decoder for 5G LDPC Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 879-891	3.9	7
95	Efficient Software Implementation of the SIKE Protocol Using New Data Representation. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	2
94	Low-complexity sphere decoding for MIMO-SCMA systems. *IET Communications*, **2021**, 15, 537-545	1.3	2
93	FTA-GAN: A Computation-Efficient Accelerator for GANs With Fast Transformation Algorithm. *IEEE Transactions on Neural Networks and Learning Systems*, **2021**, PP,	10.3	1
92	Fast Modular Multipliers for Supersingular Isogeny-Based Post-Quantum Cryptography. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 359-371	2.6	2
91	DARM: A Low-Complexity and Fast Modular Multiplier for Lattice-Based Cryptography **2021**,		2
90	High-Speed FPGA Implementation of SIKE Based on an Ultra-Low-Latency Modular Multiplier. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 3719-3731	3.9	8
89	Generalized Analog-to-Information Converter With Analysis Sparse Prior. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 3574-3586	3.9	1
88	An Improved Method for Performance Analysis of Generalized Integrated Interleaved Codes. *IEEE Communications Letters*, **2021**, 1-1	3.8	
87	CLA Formula and its Acceleration of Architecture Design for Clustered Look-Ahead Pipelined Recursive Digital Filter. *Journal of Signal Processing Systems*, **2020**, 93, 617	1.4	
86	A Precision-Scalable Energy-Efficient Convolutional Neural Network Accelerator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 3484-3497	3.9	7
85	Fine-Grained Bit-Flipping Decoding for LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 896-900	3.5	8
84	A Novel Approximation Methodology and Its Efficient VLSI Implementation for the Sigmoid Function. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3422-3426	3.5	4
83	Efficient Precision-Adjustable Architecture for Softmax Function in Deep Learning. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3382-3386	3.5	11

82	Multi-Layer Generalized Integrated Interleaved Codes. *IEEE Communications Letters*, **2020**, 24, 1880-1884	3.8	3
81	Calibration of timing mismatch in TIADC based on monotonicity detecting of sampled data. *IEICE Electronics Express*, **2020**, 17, 20190699-20190699	0.5	2
80	A Universal Approximation Method and Optimized Hardware Architectures for Arithmetic Functions Based on Stochastic Computing. *IEEE Access*, **2020**, 8, 46229-46241	3.5	6
79	Hardware Accelerator for Multi-Head Attention and Position-Wise Feed-Forward in the Transformer **2020**,		6
78	Efficient Inference of Large-Scale and Lightweight Convolutional Neural Networks on FPGA **2020**,		1
77	A Reconfigurable DNN Training Accelerator on FPGA **2020**,		1
76	A Novel Iterative Reliability-Based Majority-Logic Decoder for NB-LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1399-1403	3.5	2
75	GH CORDIC-Based Architecture for Computing N th Root of Single-Precision Floating-Point Number. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 864-875	2.6	9
74	Information Storage Bit-Flipping Decoder for LDPC Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 2464-2468	2.6	5
73	F-DNA: Fast Convolution Architecture for Deconvolutional Network Acceleration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1867-1880	2.6	4
72	A Novel Modular Multiplier for Isogeny-Based Post-Quantum Cryptography **2020**,		3
71	Hardware Accelerator for Engle-Granger Cointegration in Pairs Trading **2020**,		1
70	Optimized Trellis-Based Min-Max Decoder for NB-LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 57-61	3.5	5
69	USCA: A Unified Systolic Convolution Array Architecture for Accelerating Sparse Neural Network **2019**,		3
68	Efficient T-EMS Based Decoding Algorithms for High-Order LDPC Codes. *IEEE Access*, **2019**, 7, 50980-50992	3.5	1
67	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2156-2169	2.6	15
66	Improved Fast-SSC-Flip Decoding of Polar Codes. *IEEE Communications Letters*, **2019**, 23, 950-953	3.8	6
65	A Low-latency Sparse-Winograd Accelerator for Convolutional Neural Networks **2019**,		8

64	Analysis and Design of a Large Dither Injection Circuit for Improving Linearity in Pipelined ADCs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2008-2020	2.6	5
63	E-LSTM: An Efficient Hardware Architecture for Long Short-Term Memory. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2019**, 9, 280-291	5.2	16
62	A 124-Gb/s Decoder for Generalized Integrated Interleaved Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 3174-3187	3.9	10
61	An Improved Gradient Descent Bit-Flipping Decoder for LDPC Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 3188-3200	3.9	8
60	Improved Decoding Algorithms of LDPC Codes Based on Reliability Metrics of Variable Nodes. *IEEE Access*, **2019**, 7, 35769-35778	3.5	5
59	Modified GII-BCH Codes for Low-Complexity and Low-Latency Encoders. *IEEE Communications Letters*, **2019**, 23, 785-788	3.8	5
58	A High-Speed Successive-Cancellation Decoder for Polar Codes Using Approximate Computing. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 227-231	3.5	4
57	FPAP: A Folded Architecture for Energy-Quality Scalable Convolutional Neural Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 288-301	3.9	4
56	A New Clock Phase Calibration Method in High-Speed and High-Resolution DACs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 332-336	3.5	
55	An Efficient Post-Processor for Lowering the Error Floor of LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 397-401	3.5	2
54	Background Calibration of Comparator Offsets in SHA-Less Pipelined ADCs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 357-361	3.5	3
53	A New Probabilistic Gradient Descent Bit Flipping Decoder for LDPC Codes **2019**,		4
52	Methodology for Efficient Reconfigurable Architecture of Generative Neural Network **2019**,		4
51	TIE **2019**,		19
50	A Novel Low-Complexity Joint Coding and Decoding Algorithm for NB-LDPC Codes **2019**,		1
49	A New Fast-SSC-Flip Decoding of Polar Codes **2019**,		1
48	A Hardware-Oriented and Memory-Efficient Method for CTC Decoding. *IEEE Access*, **2019**, 7, 120681-120694	3.5	3
47	Improved Soft-Assisted Iterative Bounded Distance Decoding for Product Codes **2019**,		1

46	DynExit: A Dynamic Early-Exit Strategy for Deep Residual Networks **2019**,		1
45	Ultra-Fast Modular Multiplication Implementation for Isogeny-Based Post-Quantum Cryptography **2019**,		6
44	Corrections to Generalized Hyperbolic CORDIC and Its Logarithmic and Exponential Computation With Arbitrary Fixed Base[Sep 19 DOI: 10.1109/TVLSI.2019.2919557]. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2222-2222	2.6	0
43	Training Deep Neural Networks Using Posit Number System **2019**,		4
42	Hybrid Preconditioned CG Detection with Sequential Update for Massive MIMO Systems **2019**,		1
41	Hardware Implementation of Improved Fast-SSC-Flip Decoder for Polar Codes **2019**,		5
40	Fast-ABC: A Fast Architecture for Bottleneck-Like Based Convolutional Neural Networks **2019**,		4
39	An Improved Gauss-Seidel Algorithm and Its Efficient Architecture for Massive MIMO Systems. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1194-1198	3.5	22
38	Efficient Hardware Architectures for Deep Convolutional Neural Network. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 1941-1953	3.9	61
37	Stuck-at-close defect propagation and its blocking technique in CMOL cell mapping. *Microelectronics Journal*, **2018**, 72, 100-108	1.8	4
36	Low Complexity Message Passing Detection Algorithm for Large-Scale MIMO Systems. *IEEE Wireless Communications Letters*, **2018**, 7, 708-711	5.9	19
35	Design of Binary LDPC Codes With Parallel Vector Message Passing. *IEEE Transactions on Communications*, **2018**, 66, 1363-1375	6.9	6
34	A Stage-Combined Belief Propagation Decoder for Polar Codes. *Journal of Signal Processing Systems*, **2018**, 90, 687-694	1.4	0
33	A 21.66 Gbps Nonbinary LDPC Decoder for High-Speed Communications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 226-230	3.5	4
32	Hardware-Oriented Compression of Long Short-Term Memory for Efficient Inference. *IEEE Signal Processing Letters*, **2018**, 25, 984-988	3.2	6
31	An Efficient Convolution Core Architecture for Privacy-Preserving Deep Learning **2018**,		6
30	FPAP: A Folded Architecture for Efficient Computing of Convolutional Neural Networks **2018**,		2
29	CORDIC-Based Architecture for Computing Nth Root and Its Implementation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 4183-4195	3.9	20

28	An Energy-Efficient Architecture for Binary Weight Convolutional Neural Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 280-293	2.6	34
27	A High-Speed and Low-Complexity Architecture for Softmax Function in Deep Learning **2018**,		25
26	A Low-Complexity Decoder for Turbo Product Codes Based on Extended Hamming Codes **2018**,		1
25	Comparison between Generalized Integrated Interleaved Codes and Generalized Error Location Codes **2018**,		1
24	Fast and Low-Complexity Decoding Algorithm and Architecture for Quadruple-Error-Correcting RS codes **2018**,		3
23	Compressed Level Crossing Sampling for Ultra-Low Power IoT Devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 2495-2507	3.9	6
22	Fully-Parallel Area-Efficient Deep Neural Network Design Using Stochastic Computing. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1382-1386	3.5	17
21	A reduced complexity decoding algorithm for NB-LDPC codes **2017**,		2
20	Efficient fast convolution architectures for convolutional neural network **2017**,		8
19	Segmented successive cancellation list polar decoding with joint BCH-CRC codes **2017**,		2
18	Low-complexity detection algorithms based on matrix partition for massive MIMO **2017**,		4
17	Accelerating Recurrent Neural Networks: A Memory-Efficient Approach. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2763-2775	2.6	39
16	Efficient Soft Cancelation Decoder Architectures for Polar Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 87-99	2.6	11
15	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1159-1163	2.6	13
14	Energy efficient SVM classifier using approximate computing **2017**,		4
13	Advanced Baseband Processing Algorithms, Circuits, and Implementations for 5G Communication. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2017**, 7, 477-490	5.2	15
12	Guest Editorial Advanced Baseband Processing Circuits and Systems for 5G Communications. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2017**, 7, 473-476	5.2	
11	Algorithm and architecture for joint detection and decoding for MIMO with LDPC codes **2017**,		3

10	Reduced complexity message passing detection algorithm in large-scale MIMO systems **2017**,		1
9	Area-Efficient Scaling-Free DFT/FFT Design Using Stochastic Computing. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 1131-1135	3.5	15
8	Improved BP decoder for polar codes based on a modified kernel matrix. *Electronics Letters*, **2016**, 52, 1982-1984	1.1	1
7	Intra-layer nonuniform quantization of convolutional neural network **2016**,		5
6	Beyond 100Gbps Encoder Design for Staircase Codes **2016**,		1
5	Efficient convolution architectures for convolutional neural network **2016**,		13
4	Area-efficient check node unit architecture for single block-row quasi-cyclic LDPC codes **2014**,		1
3	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2011**, 58, 839-847	3.9	19
2	High-Throughput Layered LDPC Decoding Architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 582-587	2.6	29
1	A low latency traffic sign detection model with an automatic data labeling pipeline. *Neural Computing and Applications*,1	4.8	