

# Hyojun Kim

## List of Publications by Year in descending order

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Version: 2024-02-01

5  
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#	ARTICLE	IF	CITATIONS
1	A Low-Jitter 8-GHz RO-Based ADPLL With PVT-Robust Replica-Based Analog Closed Loop for Supply Noise Compensation. IEEE Journal of Solid-State Circuits, 2022, 57, 1712-1722.	5.4	2
2	An Adaptive Offset Cancellation Scheme and Shared-Summer Adaptive DFE for 0.068 pJ/b/dB 1.62-to-10 Gb/s Low-Power Receiver in 40 nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 622-626.	3.0	7
3	A 10 Gb/s PAM-4 Transmitter with Feed-Forward Implementation of Tomlinson-Harashima Precoding in 28 nm CMOS. IEEE Access, 2021, , 1-1.	4.2	2
4	A 0.1-pJ/b/dB 1.62-to-10.8-Gb/s Video Interface Receiver With Jointly Adaptive CTLE and DFE Using Biased Data-Level Reference. IEEE Journal of Solid-State Circuits, 2020, 55, 2186-2195.	5.4	29
5	Synthesizable glitch-free phase rotator with conditionally cascading scheme. Electronics Letters, 2020, 56, 536-538.	1.0	0