Wooheon Kang

List of Publications by Year
in descending order

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152	901	566801 15	676716 22
papers	citations	h-index	g-index

152	152	152	450
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Fast Built-in Redundancy Analysis for Memories With Optimal Repair Rate Using a Line-Based Search Tree. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1665-1678.	2.1	51
2	An Advanced BIRA for Memories With an Optimal Repair Rate and Fast Analysis Speed by Using a Branch Analyzer. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 2014-2026.	1.9	48
3	New Distributed Arithmetic Algorithm for Low-Power FIR Filter Implementation. IEEE Signal Processing Letters, 2004, 11, 463-466.	2.1	35
4	Code-Width Testing-Based Compact ADC BIST Circuit. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 603-606.	2.3	29
5	A BIRA for Memories With an Optimal Repair Rate Using Spare Memories for Area Reduction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2336-2349.	2.1	25
6	Increasing encoding efficiency of LFSR reseeding-based test compression. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 913-917.	1.9	24
7	A Lossless Color Image Compression Architecture Using a Parallel Golomb-Rice Hardware CODEC. IEEE Transactions on Circuits and Systems for Video Technology, 2011, 21, 1581-1587.	5.6	23
8	A Delay Test Architecture for TSV With Resistive Open Defects in 3-D Stacked Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2380-2387.	2.1	21
9	Hardware-Efficient Built-In Redundancy Analysis for Memory With Various Spares. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 844-856.	2.1	20
10	Proof of Concept of Home IoT Connected Vehicles. Sensors, 2017, 17, 1289.	2.1	20
11	An Efficient Hardware Architecture of the A-star Algorithm for the Shortest Path Search Engine. , 2009, , .		19
12	MDSI: Signal Integrity Interconnect Fault Modeling and Testing for SoCs. Journal of Electronic Testing: Theory and Applications (JETTA), 2007, 23, 357-362.	0.9	18
13	Total Energy Minimization of Real-Time Tasks in an On-Chip Multiprocessor Using Dynamic Voltage Scaling Efficiency Metric. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2088-2092.	1.9	18
14	A 3 Dimensional Built-In Self-Repair Scheme for Yield Improvement of 3 Dimensional Memories. IEEE Transactions on Reliability, 2015, 64, 586-595.	3.5	18
15	R²-TSV: A Repairable and Reliable TSV Set Structure Reutilizing Redundancies. IEEE Transactions on Reliability, 2017, 66, 458-466.	3.5	17
16	ATPG-XP: Test Generation for Maximal Crosstalk-Induced Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1401-1413.	1.9	16
17	A memory-efficient parallel string matching for intrusion detection systems. IEEE Communications Letters, 2009, 13, 1004-1006.	2.5	16
18	Scan Chain Reordering-Aware X-Filling and Stitching for Scan Shift Power Reduction. , 2015, , .		15

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19	A new maximal diagnosis algorithm for interconnect test. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 532-537.	2.1	14
20	EOF: Efficient Built-In Redundancy Analysis Methodology With Optimal Repair Rate. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1130-1135.	1.9	14
21	A New Fuse Architecture and a New Post-Share Redundancy Scheme for Yield Enhancement in 3-D-Stacked Memories. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 786-797.	1.9	13
22	Fault Group Pattern Matching With Efficient Early Termination for High-Speed Redundancy Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1473-1482.	1.9	13
23	Test-decompression mechanism using a variable-length multiple-polynomial LFSR. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 687-690.	2.1	12
24	A Novel Massively Parallel Testing Method Using Multi-Root for High Reliability. IEEE Transactions on Reliability, 2015, 64, 486-496.	3.5	12
25	Highly Reliable Redundant TSV Architecture for Clustered Faults. IEEE Transactions on Reliability, 2019, 68, 237-247.	3.5	12
26	A Pattern Group Partitioning for Parallel String Matching using a Pattern Grouping Metric. IEEE Communications Letters, 2010, 14, 878-880.	2.5	11
27	An ant colony optimization approach for the preference-based shortest path search. Journal of the Chinese Institute of Engineers, Transactions of the Chinese Institute of Engineers,Series A/Chung-kuo Kung Ch'eng Hsuch K'an, 2011, 34, 181-196.	0.6	11
28	A scan shifting method based on clock gating of multiple groups for low power scan testing. , 2015, , .		11
29	Grouping-Based TSV Test Architecture for Resistive Open and Bridge Defects in 3-D-ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1759-1763.	1.9	11
30	Dynamic Built-In Redundancy Analysis for Memory Repair. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2365-2374.	2.1	11
31	Fast Built-In Redundancy Analysis Based on Sequential Spare Line Allocation. IEEE Transactions on Reliability, 2018, 67, 264-273.	3.5	10
32	An efficient all-digital built-in self-test for chargepump PLL. , 0, , .		9
33	Integration of dual channel timing formatter system for high speed memory test equipment. , 2012, , .		9
34	A TSV test structure for simultaneously detecting resistive open and bridge defects in 3D-ICs. , 2016, , .		9
35	Robust Secure Shield Architecture for Detection and Protection Against Invasive Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3023-3034.	1.9	9
36	An Effective Programmable Memory BIST for Embedded Memory. IEICE Transactions on Information and Systems, 2009, E92-D, 2508-2511.	0.4	8

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37	A Scalable and Parallel Test Access Strategy for NoC-Based Multicore System. , 2014, , .		8
38	Optimized Built-In Self-Repair for Multiple Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-10.	2.1	8
39	TSV Repair Architecture for Clustered Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 190-194.	1.9	8
40	A 3-D Rotation-Based Through-Silicon via Redundancy Architecture for Clustering Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1925-1934.	1.9	8
41	A hardware-efficent multi-character string matching architecture using brute-force algorithm. , 2009, , .		7
42	A Fast Redundancy Analysis Algorithm in ATE for Repairing Faulty Memories. ETRI Journal, 2012, 34, 478-481.	1.2	7
43	Eco Assist Techniques through Real-time Monitoring of BEV Energy Usage Efficiency. Sensors, 2015, 15, 14946-14959.	2.1	7
44	Tri-State Coding Using Reconfiguration of Twisted Ring Counter for Test Data Compression. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 274-284.	1.9	7
45	An On-Chip Error Detection Method to Reduce the Post-Silicon Debug Time. IEEE Transactions on Computers, 2017, 66, 38-44.	2.4	7
46	An In-DRAM BIST for 16 Gb DDR4 DRAM in the 2nd 10-nm-Class DRAM Process. IEEE Access, 2021, 9, 33487-33497.	2.6	7
47	Fail Memory Configuration Set for RA Estimation. , 2020, , .		7
48	A New Scan Architecture for Both Low Power Testing and Test Volume Compression Under SOC Test Environment. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 365-378.	0.9	6
49	An Advanced BIRA using parallel sub-analyzers for embedded memories. , 2009, , .		6
50	Thermal-aware dynamic voltage frequency scaling for many-core processors under process variations. IEICE Electronics Express, 2013, 10, 20130463-20130463.	0.3	6
51	A new redundancy analysis algorithm using one side pivot. , 2014, , .		6
52	A New Accelerated Endurance Test for Terabit NAND Flash Memory Using Interference Effect. IEEE Transactions on Semiconductor Manufacturing, 2015, 28, 399-407.	1.4	6
53	DRAM-Based Error Detection Method to Reduce the Post-Silicon Debug Time for Multiple Identical Cores. IEEE Transactions on Computers, 2017, 66, 1504-1517.	2.4	6
54	RAIN (RAndom Insertion) Scheduling Algorithm for SoC Test. , 0, , .		5

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55	Selective scan slice repetition for simultaneous reduction of test power consumption and test data volume. IEICE Electronics Express, 2009, 6, 1432-1437.	0.3	5
56	3-D Stacked DRAM Refresh Management With Guaranteed Data Reliability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1455-1466.	1.9	5
57	An Area-Efficient BIRA With 1-D Spare Segments. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 206-210.	2.1	5
58	A low-cost concurrent TSV test architecture with lossless test output compression scheme. PLoS ONE, 2019, 14, e0221043.	1.1	5
59	An Efficient BIRA Utilizing Characteristics of Spare Pivot Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 551-561.	1.9	5
60	A New Logic Topology-Based Scan Chain Stitching for Test-Power Reduction. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3432-3436.	2.2	5
61	On-Chip Error Detection Reusing Built-In Self-Repair for Silicon Debug. IEEE Access, 2021, 9, 56443-56456.	2.6	5
62	FRESH: A New Test Result Extraction Scheme for Fast TSV Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 336-345.	1.9	4
63	GPU-Based Redundancy Analysis Using Concurrent Evaluation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 805-817.	2.1	4
64	Scan-Chain-Fault Diagnosis Using Regressions in Cryptographic Chips for Wireless Sensor Networks. Sensors, 2020, 20, 4771.	2.1	4
65	A New Low Power Test Pattern Generator using a Transition Monitoring Window based on BIST Architecture. , 2005, , .		3
66	MICRO: a new hybrid test data compression/decompression scheme. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 649-654.	2.1	3
67	High-MDSI: A High-level Signal Integrity Fault Test Pattern Generation Method for Interconnects. , 2007, , .		3
68	An Efficient Scan Chain Diagnosis Method Using a New Symbolic Simulation. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	3
69	An area efficient programmable built-in self-test for embedded memories using an extended address counter. , 2010, , .		3
70	Yield Enhancement Techniques for 3D Memories by Redundancy Sharing among All Layers. ETRI Journal, 2012, 34, 388-398.	1.2	3
71	A 2-D compaction method using macro block for post-silicon validation. , 2015, , .		3
72	A new built-in redundancy analysis algorithm based on multiple memory blocks. , 2015, , .		3

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73	An efficient built-in self-repair scheme for area reduction. , 2017, , .		3
74	A Statistic-Based Scan Chain Reordering for Energy-Quality Scalable Scan Test. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 391-403.	2.7	3
75	Test-Friendly Data-Selectable Self-Gating (DSSG). IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1972-1976.	2.1	3
76	Advanced Low Pin Count Test Architecture for Efficient Multi-Site Testing. IEEE Transactions on Semiconductor Manufacturing, 2020, 33, 391-403.	1.4	3
77	Herringbone-Based TSV Architecture for Clustered Fault Repair and Aging Recovery. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1142-1153.	1.9	3
78	Reconfigurable Scan Architecture for High Diagnostic Resolution. IEEE Access, 2021, 9, 120537-120550.	2.6	3
79	Enhanced Postbond Test Architecture for Bridge Defects Between the TSVs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1164-1177.	2.1	3
80	Reduced-Pin-Count BOST for Test-Cost Reduction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 750-761.	1.9	3
81	An Effective Hybrid Test Data Compression Method Using Scan Chain Compaction and Dictionary-Based Scheme. , 2008, , .		2
82	An effective parallel ALPG using instruction unrolling for high speed memory testing. , 2008, , .		2
83	Path delay fault diagnosis using path scoring. , 2008, , .		2
84	A BIST architecture for multiple DACs in an LTPS TFT-LCD source driver IC. , 2009, , .		2
85	A low-cost DDEM ADC structure for the testing of high-performance DACs. , 2011, , .		2
86	Interleaving Test Algorithm for Subthreshold Leakage-Current Defects in DRAM Considering the Equal Bit Line Stress. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 803-812.	2.1	2
87	Fully Programmable Memory BIST for Commodity DRAMs. ETRI Journal, 2015, 37, 787-792.	1.2	2
88	Low power scan bypass technique with test data reduction. , 2015, , .		2
89	Parallelized Network-on-Chip-Reused Test Access Mechanism for Multiple Identical Cores. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1219-1223.	1.9	2
90	Off-chip test architecture for improving multi-site testing efficiency using tri-state decoder and 3V-level encoder. , 2017, , .		2

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91	LARECD: Low area overhead and reliable error correction DMR architecture. , 2017, , .		2
92	Reconfigurable scan architecture for test power and data volume reduction. IEICE Electronics Express, 2017, 14, 20170415-20170415.	0.3	2
93	Thermal Aware Test Scheduling for NTV Circuit. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 906-910.	1.9	2
94	Test Resource Reused Debug Scheme to Reduce the Post-Silicon Debug Cost. IEEE Transactions on Computers, 2018, 67, 1835-1839.	2.4	2
95	Prediction-Based Error Correction for GPU Reliability with Low Overhead. Electronics (Switzerland), 2020, 9, 1849.	1.8	2
96	Multibank Optimized Redundancy Analysis Using Efficient Fault Collection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2739-2752.	1.9	2
97	A Secure Scan Architecture Protecting Scan Test and Scan Dump Using Skew-Based Lock and Key. IEEE Access, 2021, 9, 102161-102176.	2.6	2
98	Hardware Efficient Built-in Self-test Architecture for Power and Ground TSVs in 3D IC. , 2021, , .		2
99	SPAR: A New Test-Point Insertion Using Shared Points for Area Overhead Reduction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4939-4951.	1.9	2
100	An Effective Power Reduction Methodology for Deterministic BIST Using Auxiliary LFSR. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 591-595.	0.9	1
101	FPGA-based verification methodology of SoC-type CMOS image signal processor. , 2009, , .		1
102	FiX-compact: A new X-tolerant response compaction scheme for fixed unknown logic values. , 2010, , .		1
103	New Fault Detection Algorithm for Multi-level Cell Flash Memroies. , 2011, , .		1
104	Bit transmission error correction scheme for FlexRay based automotive communication systems. , 2013, , .		1
105	A new TSV set architecture for high reliability. , 2013, , .		1
106	An efficient RPCT (Reduced Pin Count Testing) based on test data compression using burst clock controller in 3D-IC. , 2013, , .		1
107	New Thermal-Aware Voltage Island Formation for 3D Many-Core Processors. ETRI Journal, 2015, 37, 118-127.	1.2	1
108	Chain-Based Approach for Fast Through-Silicon-Via Coupling Delay Estimation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1178-1182.	2.1	1

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109	2-D Failure Bitmap Compression Using Line Fault Marking Method. , 2018, , .		1
110	A debug scheme to improve the error identification in post-silicon validation. PLoS ONE, 2018, 13, e0202216.	1.1	1
111	Low-Power Scan Correlation-Aware Scan Cluster Reordering for Wireless Sensor Networks. Sensors, 2021, 21, 6111.	2.1	1
112	A Circular-based TSV Repair Architecture. , 2021, , .		1
113	ECMO: ECC Architecture Reusing Content-Addressable Memories for Obtaining High Reliability in DRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 781-793.	2.1	1
114	At-speed boundary-scan interconnect testing in a board with multiple system clocks. , 0, , .		0
115	A new maximal diagnosis algorithm for bus-structured systems. , 0, , .		0
116	A new maximal diagnosis algorithm for bus-structured systems. , 0, , .		0
117	An Effective Test Pattern Generation for Testing Signal Integrity. Proceedings of the Asian Test Symposium, 2006, , .	0.0	0
118	TOSCA: Total Scan Power Reduction Architecture based on Pseudo-Random Built-in Self Test Structure. Proceedings of the Asian Test Symposium, 2006, , .	0.0	0
119	An Efficient Dictionary Organization for Maximum Diagnosis. Journal of Electronic Testing: Theory and Applications (JETTA), 2006, 22, 37-48.	0.9	0
120	XPDF-ATPG: An Efficient Test Pattern Generation for Crosstalk-Induced Faults. , 2008, , .		0
121	Variable-length block nine-coded compression technique with Huffman codes and symbol merging. , 2008, , .		0
122	A New Wafer Level Latent Defect Screening Methodology for Highly Reliable DRAM Using a Response Surface Method. , 2008, , .		0
123	A Prevenient Voltage Stress Test Method for High Density Memory. , 2008, , .		0
124	Ant colony based efficient triplet calculation methodology for arithmetic built-in self test. IEICE Electronics Express, 2008, 5, 877-881.	0.3	0
125	DFT for achieving hybrid transiton delay fault test with Reduced Pin Count Testing. , 2009, , .		0
126	A High-Level Signal Integrity Fault Model and Test Methodology for Long On-Chip Interconnections. , 2009, , .		0

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127	A new scan slice encoding scheme with flexible code for test data compression. , 2010, , .		0
128	A new static test of a DAC with a built-in structure. , 2011, , .		0
129	Test scheduling using Ant Colony Optimization for 3D integrated circuits. , 2013, , .		0
130	Dynamic thermal management for 3D multicore processors under process variations. IEICE Electronics Express, 2013, 10, 20130800-20130800.	0.3	0
131	Reducing the failure bitmap size with a partial solution search tree for the low cost automatic test equipment (ATE). , 2014, , .		0
132	Recovery-enhancing task scheduling for multicore processors under NBTI impact. IEICE Electronics Express, 2014, 11, 20140324-20140324.	0.3	0
133	Reduced-code test method using sub-histograms for pipelined ADCs. IEICE Electronics Express, 2015, 12, 20150417-20150417.	0.3	0
134	Failure bitmap compression method for 3D-IC redundancy analysis. , 2015, , .		0
135	Discussion of cost-effective redundancy architectures. , 2016, , .		0
136	Test access mechaism for stack test time reduction of 3-dimensional integrated circuit. , 2016, , .		0
137	A New3-D Fuse Architecture to Improve Yield of 3-D Memories. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1.	1.9	0
138	Neural Network Reliability Enhancement Approach Using Dropout Underutilization in GPU. , 2018, , .		0
139	3D Memory Formed of Unrepairable Memory Dice and Spare Layer. , 2018, , .		0
140	W-ERA: One-Time Memory Repair with Wafer-Level Early Repair Analysis for Cost Reduction. , 2020, , .		0
141	Fine-Grained Defect Diagnosis for CMOL FPGA Circuits. IEEE Access, 2020, 8, 163140-163151.	2.6	0
142	Effective Spare Line Allocation Built-in Redundancy Analysis With Base Common Spare for Yield Improvement of 3D Memory. IEEE Access, 2021, 9, 76716-76729.	2.6	0
143	ECC-Aware Fast and Reliable Pattern Matching Redundancy Analysis for Highly Reliable Memory. IEEE Access, 2021, 9, 133274-133288.	2.6	0
144	Histogram-Based Calibration Method for Pipeline ADCs. PLoS ONE, 2015, 10, e0129736.	1.1	0

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145	A novel X-filling method for capture power reduction. IEICE Electronics Express, 2017, 14, 20171093-20171093.	0.3	0
146	A low-cost DAC BIST structure using a resistor loop. PLoS ONE, 2017, 12, e0172331.	1.1	0
147	Area Efficient Built-In Redundancy Analysis using Pre-Solutions with Various Spare Structure. , 2021, , .		0
148	Redundancy Analysis Optimization with Clustered Known Solutions for High Speed Repair. , 2020, , .		0
149	An Effective Spare Allocation Methodology for 3D Memory Repair with BIRA. , 2021, , .		0
150	A Hybrid Test Scheme for Automotive IC in Multi-site Testing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, , 1-1.	1.9	0
151	High-MDSI: A High-level Signal Integrity Fault Test Pattern Generation Method for Interconnects. Proceedings of the Asian Test Symposium, 2007, , .	0.0	0
152	Novel Error-Tolerant Voltage-Divider-Based Through-Silicon-Via Test Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 308-321.	1.9	0