Asad A Abidi

List of Publications by Year
in descending order

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31 papers	2,208 citations	471509 17 h-index	677142 22 g-index
31 all docs	31 docs citations	31 times ranked	1580 citing authors

#	Article	IF	Citations
1	Envelope Tracking Supply Modulator with Trellis-Search-Based Switching and 160-MHz Capability. IEEE Journal of Solid-State Circuits, 2022, 57, 719-733.	5.4	5
2	Design and Analysis of an Electrical Balance Duplexer With Independent and Concurrent Dual-Band TX-RX Isolation. IEEE Journal of Solid-State Circuits, 2022, 57, 1385-1396.	5.4	4
3	References Supplied on Request: Paul Brokaw's Stamp on Analog IC Design. IEEE Solid-State Circuits Magazine, 2021, 13, 28-32.	0.4	0
4	Approximate Equivalent Circuits to Understand Tradeoffs in Geometry of On-Chip Inductors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 975-988.	5.4	6
5	An Electrical Balance Duplexer for FDD Radios that Isolates TX from RX Independently in Two Bands. , 2021, , .		3
6	A Tutorial on Systematic Design of CMOS A/D Converters: Illustrated by a 10 b, 500 MS/s SAR ADC with 2 GHz RBW. , 2021, , .		4
7	Analysis and Design of a Robust, Low-Power, Inductively Coupled LSK Data Link. IEEE Journal of Solid-State Circuits, 2020, 55, 2583-2596.	5.4	8
8	Analysis and Design of Regenerative Comparators for Low Offset and Noise. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2817-2830.	5.4	46
9	Simultaneous Transmission of Up To 94-mW Self-Regulated Wireless Power and Up To 5-Mb/s Reverse Data Over a Single Pair of Coils. IEEE Journal of Solid-State Circuits, 2019, 54, 1003-1016.	5.4	29
10	Comprehensive Analysis of Distortion in the Passive FET Sample-and-Hold Circuit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1157-1173.	5.4	19
11	Self-Regulated Wireless Power and Simultaneous 5MB/S Reverse Data over One Pair of Coils. , 2018, , .		4
12	A Unified Analysis of the Signal Transfer Characteristics of a Single-Path FET-R-C Circuit. IEICE Transactions on Electronics, 2018, E101.C, 432-443.	0.6	1
13	Processes of AM-PM Distortion in Large-Signal Single-FET Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 245-260.	5.4	40
14	Design Methodology for Phase-Locked Loops Using Binary (Bang-Bang) Phase Detectors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1637-1650.	5.4	36
15	A distance-immune low-power 4-Mbps inductively-coupled bidirectional data link. , 2017, , .		3
16	FET-R-C Circuits: A Unified Treatmentâ€"Part I: Signal Transfer Characteristics of a Single-Path. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1325-1336.	5.4	30
17	FET-R-C Circuits: A Unified Treatmentâ€"Part II: Extension to Multi-Paths, Noise Figure, and Driving-Point Impedance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1337-1348.	5.4	30
18	Understanding the regenerative comparator circuit. , 2014, , .		35

#	Article	IF	Citations
19	A Multiband RF Antenna Duplexer on CMOS: Design and Performance. IEEE Journal of Solid-State Circuits, 2013, 48, 2067-2077.	5.4	81
20	Noise in Current-Commutating Passive FET Mixers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 332-344.	5.4	46
21	Phase Noise in LC Oscillators: A Phasor-Based Analysis of a General Result and of Loaded Q. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1187-1203.	5.4	105
22	Second-Order Intermodulation in Current-Commutating Passive FET Mixers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 2556-2568.	5.4	40
23	All-Digital Outphasing Modulator for a Software-Defined Transmitter. IEEE Journal of Solid-State Circuits, 2009, 44, 1260-1271.	5.4	43
24	A Low-Noise Wideband Digital Phase-Locked Loop Based on a Coarseâ€“Fine Time-to-Digital Converter With Subpicosecond Resolution. IEEE Journal of Solid-State Circuits, 2009, 44, 2808-2816.	5.4	222
25	All-digital out-phasing modulator for a software-defined transmitter. , 2008, , .		2
26	A 9 b, 1.25 ps Resolution Coarseâ€“Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies a Time Residue. IEEE Journal of Solid-State Circuits, 2008, 43, 769-777.	5.4	377
27	A low noise, wideband digital phase-locked loop based on a new time-to-digital converter with subpicosecond resolution. , 2008, , .		39
28	The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking. IEEE Journal of Solid-State Circuits, 2007, 42, 1916-1932.	5.4	234
29	A 9b, 1.25ps Resolutilon Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue. , 2007, , .		53
30	The Path to the Software-Defined Radio Receiver. IEEE Journal of Solid-State Circuits, 2007, 42, 954-966.	5.4	334
31	An 800-MHzâ€“6-GHz Software-Defined Wireless Receiver in 90-nm CMOS. IEEE Journal of Solid-State Circuits, 2006, 41, 2860-2876.	5.4	329