

# Lesley Shannon

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/5770076/publications.pdf>

Version: 2024-02-01

32  
papers

421  
citations

2257833

3  
h-index

2053595

5  
g-index

32  
all docs

32  
docs citations

32  
times ranked

391  
citing authors

| #  | ARTICLE   | IF  | CITATIONS |
|----|---|-----|-----------|
| 1  | Abigaille-III: A Versatile, Bioinspired Hexapod for Scaling Smooth Vertical Surfaces. Journal of Bionic Engineering, 2014, 11, 1-17.  | 2.7 | 67        |
| 2  | FUSE: Front-End User Framework for O/S Abstraction of Hardware Accelerators. , 2011, , .  |     | 55        |
| 3  | Amoeba-Cache: Adaptive Blocks for Eliminating Waste in the Memory Hierarchy. , 2012, , .  |     | 49        |
| 4  | Efficient PUF-Based Key Generation in FPGAs Using Per-Device Configuration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 364-375.  | 2.1 | 41        |
| 5  | TAIGA: A new RISC-V soft-processor framework enabling high performance CPU architectural features. , 2017, , .  |     | 33        |
| 6  | Coupling bio-logging with nutritional geometry to reveal novel insights into the foraging behaviour of a plunge-diving marine predator. New Zealand Journal of Marine and Freshwater Research, 2016, 50, 418-432. | 0.8 | 24        |
| 7  | Polyblaze: From one to many bringing the microblaze into the multicore era with Linux SMP support. , 2012, , .  |     | 23        |
| 8  | Scalable, High Performance Fourier Domain Optical Coherence Tomography: Why FPGAs and Not GPGPUs. , 2011, , .   |     | 18        |
| 9  | Evaluating the Performance Efficiency of a Soft-Processor, Variable-Length, Parallel-Execution-Unit Architecture for FPGAs Using the RISC-V ISA. , 2018, , .  |     | 15        |
| 10 | Technology Scaling in FPGAs: Trends in Applications and Architectures. , 2015, , .  |     | 13        |
| 11 | Rethinking Integer Divider Design for FPGA-Based Soft-Processors. , 2019, , .   |     | 13        |
| 12 | Modular Block-RAM-Based Longest-Prefix Match Ternary Content-Addressable Memories. , 2018, , .  |     | 11        |
| 13 | Supergenes in a genetic algorithm for heterogeneous FPGA placement. , 2013, , .   |     | 8         |
| 14 | Identifying and placing heterogeneously-sized cluster groupings based on FPGA placement data. , 2014, , .   |     | 7         |
| 15 | Finding System-Level Information and Analyzing Its Correlation to FPGA Placement. , 2010, , .   |     | 6         |
| 16 | A configurable framework for investigating workload execution. , 2010, , .  |     | 5         |
| 17 | Exploring FPGA technology mapping for fracturable LUT minimization. , 2011, , .   |     | 5         |
| 18 | Minimizing the error: A study of the implementation of an Integer Split-Radix FFT on an FPGA for medical imaging. , 2012, , .   |     | 5         |

| #  | ARTICLE   | IF  | CITATIONS |
|----|---|-----|-----------|
| 19 | Revisiting Deep Learning Parallelism: Fine-Grained Inference Engine Utilizing Online Arithmetic. , 2019, , .  |     | 5         |
| 20 | Bio-inspired walking: A FPGA multicore system for a legged robot. , 2012, , .   |     | 4         |
| 21 | FPGA Computing. IEEE Micro, 2021, 41, 6-7.  | 1.8 | 3         |
| 22 | A Multiprocessor System-on-Chip Implementation of a Laser-based Transparency Meter on an FPGA. , 2007, , .  |     | 2         |
| 23 | A new flexible PR domain model to replace the fixed multi-PR region model for DPR systems. , 2008, , .  |     | 2         |
| 24 | A multi-beam Scan Mode Synthetic Aperture Radar processor suitable for satellite operation. , 2016, , .   |     | 2         |
| 25 | Extending the SIMPPL SoC architectural framework to support application-specific architectures on multi-FPGA platforms. , 2008, , .                                   |     | 1         |
| 26 | An on-chip testbed that emulates runtime traffic and reduces design verification time for FPGA designs. , 2008, , .   |     | 1         |
| 27 | Facilitating Processor-Based DPR Systems for non-DPR Experts. , 2008, , .   |     | 1         |
| 28 | Exploring Writeback Designs for Efficiently Leveraging Parallel-Execution Units in FPGA-Based Soft-Processors. , 2020, , .  |     | 1         |
| 29 | Reliable Circuit Design Using a Fast Incremental-Based Gate Sizing Under Process Variation. IEEE Transactions on Device and Materials Reliability, 2022, 22, 371-380. | 1.5 | 1         |
| 30 | Customizing controller instruction sets for application-specific architectures. , 2010, , .   |     | 0         |
| 31 | Guest Editorial: Field-Programmable Technology. Journal of Signal Processing Systems, 2012, 67, 1-2.  | 1.4 | 0         |
| 32 | Future DREAMS: Dynamically Reconfigurable Extensible Architectures for Manycore Systems. , 2015, , 151-165.   |     | 0         |