# Jose G Delgado-Frias

List of Publications by Year
in descending order



| 102 | 809 | 623734 | 713466 |
|---|---|---|---|
| papers | citations | 14 h-index | 21 g-index |

| 104 | 104 | 104 | 436 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Asymmetric Crosstalk Harnessed Signaling for Large 3D Routing Integration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1059-1063. | 3.0 | 1 |
| 2 | A Crosstalk-Harnessed Signaling Enhancement that Eliminates Common-Mode Encoding. , 2021, , . | | 2 |
| 3 | Asymmetric Crosstalk Harness Signaling for Common Eigenmode Elimination. IEEE Transactions on Computers, 2021, , 1-1. | 3.4 | 1 |
| 4 | Effective Low Leakage 6T and 8T FinFET SRAMs: Using Cells With Reverse-Biased FinFETs, Near-Threshold Operation, and Power Gating. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 765-769. | 3.0 | 26 |
| 5 | Online Firmware Functional Validation Scheme Using Colored Petri Net Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1532-1545. | 2.7 | 6 |
| 6 | MWSCAS Guest Editorial Special Issue Based on the 62nd International Midwest Symposium on Circuits and Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3249-3250. | 5.4 | 0 |
| 7 | An implemented, initialization algorithm for many-dimension, Monte Carlo circuit simulations using Spice. , 2017, , . | | 3 |
| 8 | Full-VDD and near-threshold performance of 8T FinFET SRAM cells. The Integration VLSI Journal, 2017, 57, 169-183. | 2.1 | 15 |
| 9 | Firmware functional validation using a Colored Petri Net model. , 2017, , . | | 1 |
| 10 | Low-Power and Metallic-CNT-Tolerant CNTFET SRAM Design. , 2017, , 547-565. | | 0 |
| 11 | Autonomous management of a recursive area hierarchy for large scale wireless sensor networks using multiple parents. Ad Hoc Networks, 2016, 39, 1-22. | 5.5 | 2 |
| 12 | A real-time UEFI functional validation tool with behavior Colored Petri Net model. , 2016, , . | | 2 |
| 13 | UEFI USB bus initialization verification using Colored Petri Net. , 2015, , . | | 1 |
| 14 | Near-threshold CNTFET SRAM cell design with removed metallic CNT tolerance. , 2015, , . | | 3 |
| 15 | An evaluation of 6T and 8T FinFET SRAM cell leakage currents. , 2014, , . | | 4 |
| 16 | Near-Threshold CNTFET SRAM Cell Design With Word-Line Boosting and Removed Metallic CNT Tolerance. IEEE Nanotechnology Magazine, 2014, 13, 182-191. | 2.0 | 7 |
| 17 | CNTFET 8T SRAM cell performance with near-threshold power supply scaling. , 2013, , . | | 4 |
| 18 | Management of large-scale wireless sensor networks utilizing multi-parent recursive area hierarchies. , 2013, , . | | 1 |

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|---|---|---|---|
| 19 | Near-threshold CNTFET SRAM cell design with gated cell power supply. , 2013, , . | | 3 |
| 20 | SRAM leakage in CMOS, FinFET and CNTFET technologies. , 2012, , . | | 14 |
| 21 | NOA: A Scalable Multi-Parent Clustering Hierarchy for WSNs. Procedia Computer Science, 2012, 10, 1140-1145. | 2.0 | 2 |
| 22 | FinFET 3T and 3T1D dynamic RAM cells. , 2012, , . | | 4 |
| 23 | A superscalar processor for a medium-grain reconfigurable hardware. , 2012, , . | | 0 |
| 24 | Carbon Nanotube SRAM Design With Metallic CNT or Removed Metallic CNT Tolerant Approaches. IEEE Nanotechnology Magazine, 2012, 11, 788-798. | 2.0 | 26 |
| 25 | CNTFET SRAM cell with tolerance to removed metallic CNTs. , 2012, , . | | 3 |
| 26 | Low power and metallic CNT tolerant CNTFET SRAM design. , 2011, , . | | 8 |
| 27 | CNTFET gate design with tolerance to metallic CNTs. , 2011, , . | | 2 |
| 28 | Performance-power tradeoffs of 8T FinFET SRAM cells. , 2011, , . | | 4 |
| 29 | A performance-power evaluation of FinFET flip-flops under process variations. , 2011, , . | | 0 |
| 30 | A medium-grain reconfigurable processor organization. , 2011, , . | | 2 |
| 31 | FPGA schemes for minimizing the power-throughput trade-off in executing the Advanced Encryption Standard algorithm. Journal of Systems Architecture, 2010, 56, 116-123. | 4.3 | 31 |
| 32 | A novel analytical model for wormhole switching network on chip with adaptive routing. , 2010, , . | | 2 |
| 33 | A medium-grain reconfigurable processing unit. , 2010, , . | | 2 |
| 34 | Low power SRAM cell design for FinFET and CNTFET technologies. , 2010, , . | | 16 |
| 35 | CNTFET SRAM cell design with tolerance to metallic CNTs. , 2010, , . | | 4 |
| 36 | Low-Power FinFET design schemes for NOR address decoders. , 2010, , . | | 6 |

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| 37 | IP Routing table compaction and sampling schemes to enhance TCAM cache performance. Journal of Systems Architecture, 2009, 55, 61-69. | 4.3 | 5 |
| 38 | Decreasing energy consumption in address decoders by means of selective precharge schemes. Microelectronics Journal, 2009, 40, 1590-1600. | 2.0 | 7 |
| 39 | Performance of CNFET SRAM cells under diameter variation corners. , 2009, , . | | 8 |
| 40 | Delay and Energy Analysis of SEU and SET-Tolerant Pipeline Latches and Flip-Flops. IEEE Transactions on Nuclear Science, 2009, 56, 1618-1628. | 2.0 | 26 |
| 41 | Intelligent management of distributed dynamic sensor networks. Artificial Life and Robotics, 2008, 12, 81-87. | 1.2 | 8 |
| 42 | High-Performance Low-Power Selective Precharge Schemes for Address Decoders. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 917-921. | 3.0 | 18 |
| 43 | Multiple node upset mitigation in TPDICE-based pipeline memory structures. , 2008, , . | | 0 |
| 44 | A Medium-Grain Reconfigurable Architecture for DSP: VLSI Design, Benchmark Mapping, and Performance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 14-23. | 3.1 | 17 |
| 45 | Clock skew tolerant communication scheme for SoC IP blocks. , 2008, , . | | 1 |
| 46 | High-performance low-power AND and Sense-Amp address decoders with selective precharging. , 2008, , . | | 2 |
| 47 | Reducing power in memory decoders by means of selective precharge schemes. Midwest Symposium on Circuits and Systems, 2007, , . | 1.0 | 5 |
| 48 | Using a Cache Scheme to Detect Misbehaving Nodes in Mobile Ad-Hoc Networks. Networks, 2008 ICON 2008 16th IEEE International Conference on, 2007, , . | 0.0 | 3 |
| 49 | Hardened by Design Techniques for Implementing Multiple-Bit Upset Tolerant Static Memories. , 2007, , . | | 23 |
| 50 | MARS: Misbehavior Detection in Ad Hoc Networks. , 2007, , . | | 14 |
| 51 | Medium-Grain Cells for Reconfigurable DSP Hardware. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1255-1265. | 0.1 | 9 |
| 52 | Redundant Array of Independent Fabrics - An Architecture for Next Generation Network. , 2007, , . | | 0 |
| 53 | Fault Tolerant Interleaved Switching Fabrics For Scalable High-Performance Routers. IEEE Transactions on Parallel and Distributed Systems, 2007, 18, 1727-1739. | 5.6 | 14 |
| 54 | A two-level reconfigurable architecture for digital signal processing. Microelectronic Engineering, 2007, 84, 244-252. | 2.4 | 10 |

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| 55 | Preface of Special Issue on VLSI Design and Test. Microelectronic Engineering, 2007, 84, 193. | 2.4 | 2 |
| 56 | Emergent societies: advanced IT support of crisis relief missions. Artificial Life and Robotics, 2007, 11, 116-122. | 1.2 | 2 |
| 57 | NXG05-1: Interleaved Multistage Switching Fabrics for Scalable High Performance Routers. IEEE Global Telecommunications Conference (GLOBECOM), 2006, , . | 0.0 | 2 |
| 58 | Schemes for eliminating transient-width clock overhead from SET-tolerant memory-based systems. IEEE Transactions on Nuclear Science, 2006, 53, 1564-1573. | 2.0 | 27 |
| 59 | A Shared Self-Compacting Buffer for Network-On-Chip Systems. Midwest Symposium on Circuits and Systems, 2006, , . | 1.0 | 10 |
| 60 | A mesochronous pipelining scheme for high-performance digital systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 1078-1088. | 0.1 | 10 |
| 61 | An Energy-Efficient Differential Flip-Flop for Deeply Pipelined Systems. Midwest Symposium on Circuits and Systems, 2006, , . | 1.0 | 12 |
| 62 | A Reduced Clock Delay Approach for High Performance Mesochronous Pipeline. Midwest Symposium on Circuits and Systems, 2006, , . | 1.0 | 1 |
| 63 | High Performance Memory Read Using Cross-Coupled Pull-up Circuitry. Midwest Symposium on Circuits and Systems, 2006, , . | 1.0 | 5 |
| 64 | Wave-Pipelining the Global Interconnect to Reduce the Associated Delays. Midwest Symposium on Circuits and Systems, 2006, , . | 1.0 | 3 |
| 65 | Performance Analysis of Multipath Data Transmission in Multihop Ad Hoc Networks. , 2006, , . | | 0 |
| 66 | Advanced IT support of crisis relief missions. Journal of Emergency Management, 2006, 4, 29-36. | 0.3 | 10 |
| 67 | Decoupled dynamic ternary content addressable memories. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 2139-2147. | 0.1 | 15 |
| 68 | A VLSI crossbar switch with wrapped wave front arbitration. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 135-141. | 0.1 | 8 |
| 69 | A hybrid wave pipelined network router. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2002, 49, 1764-1772. | 0.1 | 28 |
| 70 | A VLSI wrapped wave front arbiter for crossbar switches. , 2001, , . | | 2 |
| 71 | BASIS: A Biological Approach to System Information Security. Lecture Notes in Computer Science, 2001, , 127-142. | 1.3 | 9 |
| 72 | A wave-pipelined router architecture using ternary associative memory. , 2000, , . | | 1 |

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| 73 | A high-performance encoder with priority lookahead. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2000, 47, 1390-1393. | 0.1 | 26 |
| 74 | Elementary function generators for neural-network emulators. IEEE Transactions on Neural Networks, 2000, 11, 1438-1449. | 4.2 | 31 |
| 75 | A neuro-emulator with embedded capabilities for generalized learning. Journal of Systems Architecture, 1999, 45, 1219-1243. | 4.3 | 1 |
| 76 | Executing tree routing algorithms on a high-performance pattern associative router. Journal of Systems Architecture, 1998, 44, 849-866. | 4.3 | 1 |
| 77 | A CLUSTERING AND GENETIC SCHEME FOR LARGE TSP OPTIMIZATION PROBLEMS. Cybernetics and Systems, 1998, 29, 137-157. | 2.5 | 3 |
| 78 | A programmable dynamic interconnection network router with hidden refresh. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1998, 45, 1182-1190. | 0.1 | 14 |
| 79 | Sigmoid generators for neural computing using piecewise approximations. IEEE Transactions on Computers, 1996, 45, 1045-1049. | 3.4 | 82 |
| 80 | Software Metrics and Microcode: A Case Study. Journal of Software: Evolution and Process, 1996, 8, 199-224. | 0.4 | 3 |
| 81 | A flexible bit-pattern associative router for interconnection networks. IEEE Transactions on Parallel and Distributed Systems, 1996, 7, 477-485. | 5.6 | 21 |
| 82 | A pattern-associative router for interconnection network adaptive algorithms. Lecture Notes in Computer Science, 1996, , 213-217. | 1.3 | 0 |
| 83 | Flexible oblivious router architecture. IBM Journal of Research and Development, 1995, 39, 315-329. | 3.1 | 8 |
| 84 | A VLSI Pipelined Neuroemulator. , 1994, , 71-80. | | 3 |
| 85 | SPIN: THE SEQUENTIAL PIPELINED NEUROEMULATOR. International Journal on Artificial Intelligence Tools, 1993, 02, 117-132. | 1.0 | 2 |
| 86 | SEMANTIC NETWORK ARCHITECTURES: AN EVALUATION. International Journal on Artificial Intelligence Tools, 1992, 01, 57-83. | 1.0 | 2 |
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| 88 | ARCHITECTURAL SCHEMES FOR SEMANTIC NETWORKS. , 1992, , 516-540. | | 0 |
| 89 | A Dataflow Architecture for AI. , 1991, , 23-32. | | 1 |
| 90 | Parallel architectures for AI semantic network processing. Knowledge-Based Systems, 1988, 1, 259-265. | 7.1 | 8 |

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| 91 | Design and evaluation of a DAMQ multiprocessor network with self-compacting buffers. , 0, , . | | 20 |
| 92 | A high performance pattern associative oblivious router for tree topologies. , 0, , . | | 5 |
| 93 | A VLSI self-compacting buffer for DAMQ communication switches. , 0, , . | | 4 |
| 94 | A dictionary machine emulation on a VLSI computing tree system. , 0, , . | | 0 |
| 95 | A VLSI high-performance encoder with priority lookahead. , 0, , . | | 16 |
| 96 | Self-timed refreshing approach for dynamic memories. , 0, , . | | 3 |
| 97 | A hybrid wave-pipelined network router. , 0, , . | | 3 |
| 98 | Pipelined multipliers for reconfigurable hardware. , 0, , . | | 5 |
| 99 | Enhanced fault-tolerant CMOS memory elements. , 0, , . | | 2 |
| 100 | A Distributed FIFO Scheme for on Chip Communication. , 0, , . | | 2 |
| 101 | A High Performance Hybrid Wave-Pipelined Multiplier. , 0, , . | | 4 |
| 102 | A mesochronous pipeline scheme for high performance low power digital systems. , 0, , . | | 1 |