Yong-Bin Kim

List of Publications by Year
in descending order

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107 papers	1,596 citations	686830 13 h-index	525886 27 g-index
108 all docs	108 docs citations	108 times ranked	972 citing authors

#	Article	IF	Citations
1	CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits. IEEE Nanotechnology Magazine, 2011, 10, 217-225.	1.1	430
2	Design of a Ternary Memory Cell Using CNTFETs. IEEE Nanotechnology Magazine, 2012, 11, 1019-1025.	1.1	116
3	Design of a CNTFET-Based SRAM Cell by Dual-Chirality Selection. IEEE Nanotechnology Magazine, 2010, 9, 30-37.	1.1	86
4	A CMOS Subbandgap Reference Circuit With 1-V Power Supply Voltage. IEEE Journal of Solid-State Circuits, 2004, 39, 252-255.	3.5	64
5	Standby Leakage Power Reduction Technique for Nanoscale CMOS VLSI Systems. IEEE Transactions on Instrumentation and Measurement, 2010, 59, 1127-1133.	2.4	63
6	A novel sort error hardened 10T SRAM cells for low voltage operation. , 2012, , .		59
7	A 11-Transistor Nanoscale CMOS Memory Cell for Hardening to Soft Errors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 900-904.	2.1	58
8	A novel design methodology to optimize the speed and power of the CNTFET circuits. , 2009, , .		54
9	A novel low-power, low-offset, and high-speed CMOS dynamic latched comparator. Analog Integrated Circuits and Signal Processing, 2012, 70, 337-346.	0.9	51
10	A new SRAM cell design using CNTFETs. , 2008, , .		43
11	Fault Tolerant Source Routing for Network-on-chip. , 2007, , .		40
12	Low power CMOS electronic central pattern generator design for a biomimetic underwater robot. Neurocomputing, 2007, 71, 284-296.	3.5	39
13	A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 517-528.	2.1	39
14	A low-offset high-speed double-tail dual-rail dynamic latched comparator. , 2010, , .		20
15	Accurate and Efficient On-Chip Spectral Analysis for Built-In Testing and Calibration Approaches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 497-506.	2.1	20
16	A Highly-Stable Nanometer Memory for Low-Power Design. , 2008, , .		18
17	Hybrid CMOS and CNFET Power Gating in Ultralow Voltage Design. IEEE Nanotechnology Magazine, 2011, 10, 1439-1448.	1.1	18
18	A high-efficiency fully digital synchronous buck converter power delivery system based on a finite-state machine. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 229-240.	2.1	17

#	Article	IF	Citations
19	A 12-bit digitally controlled oscillator with low power consumption. , 2008, , .		17
20	A low power 8T SRAM cell design technique for CNFET. , 2008, , .		15
21	A Low-Power Digitally Controlled Oscillator for All Digital Phase-Locked Loops. VLSI Design, 2010, 2010, 1-11.	0.5	15
22	A low power 100MΩ CMOS front-end transimpedance amplifier for biosensing applications. , 2010, , .		14
23	High speed and low power transceiver design with CNFET and CNT bundle interconnect. , 2010, , .		13
24	Asynchronous Advanced Encryption Standard Hardware with Random Noise Injection for Improved Side-Channel Attack Resistance. Journal of Electrical and Computer Engineering, 2014, 2014, 1-13.	0.6	12
25	Design of enhanced differential cascode voltage switch logic (EDCVSL) circuits for high fan-in gate. , 0, , .		11
26	Optimal Body Biasing for Minimum Leakage Power in Standby Mode. , 2007, , .		11
27	New SRAM Cell Design for Low Power and High Reliability Using 32nm Independent Gate FinFET Technology. , 2008, , .		10
28	Noise Reduction Technique Through Bandwidth Switching for Switched-Capacitor Amplifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1707-1715.	3.5	10
29	Circuit implementation of FitzHugh-Nagumo neuron model using Field Programmable Analog Arrays. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	9
30	A 10-Gb/s receiver with a continuous-time linear equalizer and 1-tap decision-feedback equalizer. , 2015, , .		9
31	A Two-Parameter Calibration Technique Tracking Temperature Variations for Current Source Mismatch. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 387-391.	2.2	9
32	Ultra-low voltage high-speed Schmitt trigger circuit in SOI MOSFET technology. IEICE Electronics Express, 2007, 4, 606-611.	0.3	8
33	A CMOS Low-Power Digital Polar Modulator System Integration for WCDMA Transmitter. IEEE Transactions on Industrial Electronics, 2012, 59, 1154-1160.	5.2	8
34	A high speed low power modulo 2ⁿ+1 multiplier design using carbon-nanotube technology. , 2012, , .		8
35	Low power Null Convention Logic circuit design based on DCVSL. , 2013, , .		8
36	On the modeling and analysis of jitter in ATE using Matlab. , 0, , .		7

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37	A novel technique to minimize standby leakage power in nanoscale CMOS VLSI. , 2009, , .		7
38	Design and performance measurement of efficient IDEA (International Data Encryption Algorithm) crypto-hardware using novel modular arithmetic components. , 2010, , .		7
39	The novel Switched-Capacitor DC-DC converter for fast response time and reduced ripple. , 2011, , .		7
40	Low power, high PVT variation tolerant central pattern generator design for a bio-hybrid micro robot. , 2012, , .		7
41	Jitter Analysis of PWM Scheme in High Speed Serial Link. , 2006, , .		6
42	Low power 8T SRAM using 32nm independent gate FinFET technology. , 2008, , .		6
43	A novel design technique for soft error hardening of Nanoscale CMOS memory. , 2009, , .		6
44	A 12-bit 32MS/s SAR ADC using built-in self calibration technique to minimize capacitor mismatch. , 2014, , .		6
45	A localized self-resetting gate design methodology for low power. , 0, , .		5
46	A test-vector generation methodology for crosstalk noise faults. , 0, , .		5
47	Data dependent jitter (DDJ) characterization methodology. , 0, , .		5
48	Standby power reduction using optimal supply voltage and body-bias voltage. IEICE Electronics Express, 2008, 5, 556-561.	0.3	5
49	A novel all-digital phase-locked loop with ultra fast frequency and phase acquisition. , 2009, , .		5
50	A built-in calibration system to optimize third-order intermodulation performance of RF amplifiers. , 2014, , .		5
51	Fully Integrated on-Chip Switched DCâ€“DC Converter for Battery-Powered Mixed-Signal SoCs. Symmetry, 2017, 9, 18.	1.1	5
52	A Novel Hardened Design of a CMOS Memory Cell at 32nm. , 2009, , .		4
53	Modelling a CNTFET with Undeposited CNT Defects. , 2010, , .		4
54	A 65nm CMOS ultra low power and low noise 131M front-end transimpedance amplifier. , 2010, , .		4

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55	Random dynamic voltage scaling design to enhance security of NCL S-box. , 2011, , .		4
56	A low power 65nm CMOS electronic neuron and synapse design for a biomimetic micro-robot. , 2011, , .		4
57	All-digital phased-locked loop with local passive interpolation time-to-digital converter based on a tristate inverter. , 2012, , .		4
58	Soft error masking latch for sub-threshold voltage operation. , 2012, , .		4
59	Calibration technique tracking temperature for current-steering digital-to-analog converters. , 2014, , .		4
60	A novel digital controlled technique for operational amplifier compensation. , 0, , .		3
61	Accurate Macro-modeling for Leakage Current for IDDQ Test. Conference Record - IEEE Instrumentation and Measurement Technology Conference, 2007, , .	0.0	3
62	Analysis and Simulation of Jitter for High Speed Channels in VLSI Systems. Conference Record - IEEE Instrumentation and Measurement Technology Conference, 2007, , .	0.0	3
63	Asynchronous circuit design using new high speed NCL gates. , 2014, , .		3
64	A deep sub-micron SRAM cell design and analysis methodology. , 0, , .		2
65	Implementation of a 1 volt supply voltage CMOS subbandgap reference circuit. , 0, , .		2
66	Environmental-Based Characterization of SoC-Based Instrumentation Systems for Stratified Testing. IEEE Transactions on Instrumentation and Measurement, 2005, 54, 1241-1248.	2.4	2
67	A CMOS Low Power Fully Digital Adaptive Power Delivery System Based on Finite State Machine Control. , 2007, , .		2
68	Statistical timing and leakage power analysis of PD-SOI digital circuits. Analog Integrated Circuits and Signal Processing, 2009, 60, 127-136.	0.9	2
69	Errors in DNA Self-Assembly by Synthesized Tile Sets. , 2009, , .		2
70	A novel self-calibration scheme for 12-bit 50MS/s SAR ADC. , 2014, , .		2
71	A built-in calibration system with a reduced FFT engine for linearity optimization of low power LNA. , 2014, , .		2
72	An Area Efficient 4Gb/s Half-Rate 3-Tap DFE with Current-Integrating Summer for Data Correction. , 2016, , .		2

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73	A quarter-rate 3-tap DFE for 4Gbps data rate with switched-capapctiors based 1st speculative tap. , 2017, , .		2
74	An investigation into adiabatic circuits. , 0, , .		1
75	Power Estimation in Digital CMOS VLSI Chips. , 0, , .		1
76	Wave Pipelined Circuits Synthesis. , 0, , .		1
77	Low power CMOS adaptive electronic central pattern generator design. , 2005, , .		1
78	A power optimization method to design Butterworth filter on SiGe process. , 2005, , .		1
79	A novel delay balancing methodology for wave pipelined circuits. , 2005, , .		1
80	ASLIC: A Low Power CMOS Analog Circuit Design Automation. , 0, , .		1
81	Statistical Characterization of Partially-Depleted SOI Gates. Conference Record - IEEE Instrumentation and Measurement Technology Conference, 2006, , .	0.0	1
82	A low power CMOS CORDIC processor design for wireless telecommunication. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	1
83	Probabilistic analysis of design mapping in asynchronous nanowire crossbar architecture. , 2009, , .		1
84	A novel 4-to-3 step-down on-chip SC DC-DC converter with reduced bottom-plate loss. , 2012, , .		1
85	A design and integration of Parametric Measurement Unit on to a 600MHz DCL. , 2012, , .		1
86	A 10-bit 64MS/s SAR ADC using variable clock period method. , 2013, , .		1
87	Implementation of CMOS neuron for robot motion control unit. , 2013, , .		1
88	A low power high resolution digital PWM with process and temperature calibrations for digital controlled DC-DC converters. , 2014, , .		1
89	A low jitter PLL design using active loop filter and low-dropout regulator for supply regulation. , 2015, , .		1
90	Design flow of robust routed power distribution for low power ASIC. , 0, , .		0

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91	A fast and precise interconnect capacitive coupling noise model. , 0, , .		0
92	Clock Grid Simulation using Transient S-parameter Modeling. Conference Record - IEEE Instrumentation and Measurement Technology Conference, 2006, , .	0.0	0
93	Energy efficient PWAM transmitter design. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	0
94	Monomer Control for Error Tolerance in DNA Self-Assembly. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 271-284.	0.9	0
95	An all-digital phase-locked loop with fast acquisition and low jitter. , 2008, , .		0
96	Ultra low-voltage Delay Locked Loop using carbon nanotubes. , 2010, , .		0
97	Design and analysis of a quad-ferential ampilifer. , 2011, , .		0
98	Configurable logic block (CLB) design for Asynchronous Nanowire Crossbar system. , 2012, , .		0
99	Post-configuration repair strategy for asynchronous nanowire crossbar system. , 2012, , .		0
100	Design and evaluation of Side Channel Attack resistant asynchronous AES Round Function. , 2012, , .		0
101	A high performance modulo 2ⁿ+1 squarer design based on carbon nanotube technology. , 2013, , .		0
102	Full custom implementation of a S-Box circuit architecture using power gated PLA structure. , 2014, , .		0
103	Global clock distribution using standing wave resonant on transmission lines. , 2015, , .		0
104	Time-domain temperature sensor based on interlaced hysteresis delay cells. , 2017, , .		0
105	Low Power Digital Temperature Sensor Using Modified Inverter Interlaced Cascaded Delay Cell. , 2018, , .		0
106	Area Efficient 4Gb/s Clock Data Recovery Using Improved Phase Interpolator with Error Monitor. , 2018, , .		0
107	A Tunable High-Gain Low-Noise Transimpedance Amplifier for Biosensing. , 2020, , .		0