Wenjuan Lu

List of Publications by Year
in descending order

17	146	1478505 6	1199594 12
papers	citations	h-index	g-index

18	18	18	115
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	In-Memory Computing With Double Word Lines and Three Read Ports for Four Operands. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1316-1320.	3.1	27
2	Cascade Current Mirror to Improve Linearity and Consistency in SRAM In-Memory Computing. IEEE Journal of Solid-State Circuits, 2021, 56, 2550-2562.	5.4	24
3	Average 7T1R Nonvolatile SRAM With R/W Margin Enhanced for Low-Power Application. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 584-588.	3.1	22
4	Readâ€decoupled 8T1R nonâ€volatile SRAM with dualâ€mode option and high restore yield. Electronics Letters, 2019, 55, 519-521.	1.0	10
5	Efficient replica bitline technique for variationâ€tolerant timing generation scheme of SRAM sense amplifiers. Electronics Letters, 2015, 51, 742-743.	1.0	8
6	An 8T SRAM Array with Configurable Word Lines for In-Memory Computing Operation. Electronics (Switzerland), 2021, 10, 300.	3.1	8
7	Impact of native defects and impurities in mâ^'HfO₂ and Î²â^'Si₃N₄ on charge trapping memory devices: A first principle hybrid functional study. Physica Status Solidi (B): Basic Research, 2017, 254, 1600360.	1.5	6
8	The study about the resistive switching based on graphene/NiO interfaces. AIP Advances, 2017, 7, 085308.	1.3	6
9	Research on c-HfO2 (0 0 1)/Î±-Al2O3 (1 -1 0 2) interface in CTM devices based on first principle theory. AIP Advances, 2017, 7, 125001.	1.3	6
10	Current mirrorâ€based compensation circuit for multiâ€row read inâ€memory computing. Electronics Letters, 2019, 55, 1176-1178.	1.0	6
11	In-Memory Multibit Multiplication Based on Bitline Shifting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 354-358.	3.0	6
12	Read/write margin enhanced 10T SRAM for low voltage application. IEICE Electronics Express, 2016, 13, 20160382-20160382.	0.8	5
13	Configurable Memory With a Multilevel Shared Structure Enabling In-Memory Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 566-578.	3.1	5
14	A novel cascade control replica-bitline delay technique for reducing timing process-variation of SRAM sense amplifier. IEICE Electronics Express, 2015, 12, 20150102-20150102.	0.8	4
15	Variation-resilient pipelined timing tracking circuit for SRAM sense amplifier. IEICE Electronics Express, 2016, 13, 20150951-20150951.	0.8	3
16	Study of the Non-Linearity on TiO₂(0 0 1) Surface with Oxygen Defects: A First-Principles Study. Nano, 2017, 12, 1750097.	1.0	0
17	A first-principles study of interfacial fluorination at the HfO2/Al2O3 interface in charge trapping memory devices. Journal of Applied Physics, 2019, 125, 215303.	2.5	0