Christoforos G Theodorou

List of Publications by Year
in descending order

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63	612	567281 15	713466 21
papers	citations	h-index	g-index

63	63	63	615
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction. Solid-State Electronics, 2015, 111, 123-128.	1.4	42
2	Low-Frequency Noise Sources in Advanced UTBB FD-SOI MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 1161-1167.	3.0	40
3	Origin of Low-Frequency Noise in the Low Drain Current Range of Bottom-Gate Amorphous IGZO Thin-Film Transistors. IEEE Electron Device Letters, 2011, 32, 898-900.	3.9	29
4	Comparison for 1/ ${f}$ Noise Characteristics of AlGaN/GaN FinFET and Planar MISHFET. IEEE Transactions on Electron Devices, 2017, 64, 3634-3638.	3.0	29
5	Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications. IEEE Transactions on Electron Devices, 2020, 67, 4563-4567.	3.0	27
6	Impact of Sourceâ€“Drain Series Resistance on Drain Current Mismatch in Advanced Fully Depleted SOI n-MOSFETs. IEEE Electron Device Letters, 2015, 36, 433-435.	3.9	25
7	Drain-Current Flicker Noise Modeling in nMOSFETs From a 14-nm FDSOI Technology. IEEE Transactions on Electron Devices, 2015, 62, 1574-1579.	3.0	23
8	All Operation Region Characterization and Modeling of Drain and Gate Current Mismatch in 14-nm Fully Depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 2080-2085.	3.0	22
9	Symmetrical unified compact model of short-channel double-gate MOSFETs. Solid-State Electronics, 2012, 69, 55-61.	1.4	19
10	Analytical Modeling of Threshold Voltage and Interface Ideality Factor of Nanoscale Ultrathin Body and Buried Oxide SOI MOSFETs With Back Gate Control. IEEE Transactions on Electron Devices, 2014, 61, 969-975.	3.0	19
11	Evolution of low frequency noise and noise variability through CMOS bulk technology nodes from 0.5Î¼m down to 20nm. Solid-State Electronics, 2014, 95, 28-31.	1.4	18
12	Effect of Gate Structure on the Trapping Behavior of GaN Junctionless FinFETs. IEEE Electron Device Letters, 2020, 41, 832-835.	3.9	18
13	Low frequency noise variability in ultra scaled FD-SOI n-MOSFETs: Dependence on gate bias, frequency and temperature. Solid-State Electronics, 2016, 117, 88-93.	1.4	17
14	Origin of the low-frequency noise in n-channel FinFETs. Solid-State Electronics, 2013, 82, 21-24.	1.4	16
15	Analytical Compact Model for Lightly Doped Nanoscale Ultrathin-Body and Box SOI MOSFETs With Back-Gate Control. IEEE Transactions on Electron Devices, 2015, 62, 3117-3124.	3.0	16
16	Low-Frequency Noise Characteristics of GaN Nanowire Gate-All-Around Transistors With/Without 2-DEG Channel. IEEE Transactions on Electron Devices, 2019, 66, 1243-1248.	3.0	16
17	Restricted Channel Migration in 2D Multilayer ReS₂. ACS Applied Materials & Interfaces, 2021, 13, 19016-19022.	8.0	13
18	Impact of front-back gate coupling on low frequency noise in 28 nm FDSOI MOSFETs. , 2012, , .		12

#	Article	IF	Citations
19	New LFN and RTN analysis methodology in 28 and 14nm FD-SOI MOSFETs. , 2015, , .		11
20	Hot carrier degradation modeling of short-channel n-FinFETs suitable for circuit simulators. Microelectronics Reliability, 2016, 56, 10-16.	1.7	11
21	Flicker noise in n-channel nanoscale tri-gate fin-shaped field-effect transistors. Applied Physics Letters, 2012, 101, .	3.3	10
22	Short Channel Effects on LTPS TFT Degradation. Journal of Display Technology, 2013, 9, 747-754.	1.2	10
23	Statistical analysis of dynamic variability in 28nm FD-SOI MOSFETs. , 2014, , .		9
24	Intermittency-induced criticality in the random telegraph noise of nanoscale UTBB FD-SOI MOSFETs. Microelectronic Engineering, 2019, 216, 111027.	2.4	9
25	Front-back gate coupling effect on 1/f noise in ultra-thin Si film FDSOI MOSFETs. , 2012, , .		8
26	Study of Hot-Carrier-Induced Traps in Nanoscale UTBB FD-SOI MOSFETs by Low-Frequency Noise Measurements. IEEE Transactions on Electron Devices, 2016, , 1-7.	3.0	8
27	Analytical low-frequency noise model in the linear region of lightly doped nanoscale double-gate metal-oxide-semiconductor field-effect transistors. Journal of Applied Physics, 2010, 108, 064512.	2.5	7
28	Low-frequency noise behavior of n-channel UTBB FD-SOI MOSFETs. , 2013, , .		7
29	Characterization and Modeling of NBTI in Nanoscale UltraThin Body UltraThin Box FD-SOI MOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 4913-4918.	3.0	7
30	Hot-carrier degradation model for nanoscale ultra-thin body ultra-thin box SOI MOSFETs suitable for circuit simulators. Microelectronic Engineering, 2016, 159, 9-16.	2.4	7
31	Chaotic Behavior of Random Telegraph Noise in Nanoscale UTBB FD-SOI MOSFETs. IEEE Electron Device Letters, 2017, 38, 517-520.	3.9	7
32	Static and Low Frequency Noise Characterization of InGaAs MOSFETs and FinFETs on Insulator. , 2018, , .		7
33	1/f noise analysis in high mobility polymer-based OTFTs with non-fluorinated dielectric. Applied Physics Letters, 2019, 114, .	3.3	7
34	Effects of Contact Potential and Sidewall Surface Plane on the Performance of GaN Vertical Nanowire MOSFETs for Low-Voltage Operation. IEEE Transactions on Electron Devices, 2020, 67, 1547-1552.	3.0	7
35	Impact of Hot Carrier Aging on the 1/f and Random Telegraph Noise of Short-Channel Triple-Gate Junctionless MOSFETs. IEEE Transactions on Device and Materials Reliability, 2021, 21, 348-353.	2.0	7
36	Impact of lowâ€frequency noise variability on statistical parameter extraction in ultraâ€scaled CMOS devices. Electronics Letters, 2014, 50, 1393-1395.	1.0	6

#	Article	IF	Citations
37	Noise and Fluctuations in Fully Depleted Silicon-on-Insulator MOSFETs. , 2020, , 33-85.		6
38	Origin of Low-Frequency Noise in Triple-Gate Junctionless n-MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 5481-5486.	3.0	5
39	Impact of Hot Carrier Aging on the Performance of Triple-Gate Junctionless MOSFETs. IEEE Transactions on Electron Devices, 2020, 67, 424-429.	3.0	5
40	A Method for Series-Resistance-Immune Extraction of Low-Frequency Noise Parameters in Nanoscale MOSFETs. IEEE Transactions on Electron Devices, 2020, 67, 4568-4572.	3.0	5
41	Low frequency noise statistical characterization of 14nm FDSOI technology node. , 2015, , .		4
42	Noise-induced dynamic variability in nano-scale CMOS SRAM cells. , 2016, , .		4
43	Static and low frequency noise characterization of ultra-thin body InAs MOSFETs. Solid-State Electronics, 2018, 143, 56-61.	1.4	4
44	Upgrade of Drain Current Compact Model for Nanoscale Triple-Gate Junctionless Transistors to Continuous and Symmetric. IEEE Transactions on Electron Devices, 2019, 66, 4486-4489.	3.0	4
45	Optimization of GOPS-Based Functionalization Process and Impact of Aptamer Grafting on the Si Nanonet FET Electrical Properties as First Steps towards Thrombin Electrical Detection. Nanomaterials, 2020, 10, 1842.	4.1	4
46	Dynamic variability in 14nm FD-SOI MOSFETs and transient simulation methodology. Solid-State Electronics, 2015, 111, 100-103.	1.4	3
47	Drain current local variability from linear to saturation region in 28nm bulk NMOSFETs. , 2016, , .		3
48	Drain current local variability from linear to saturation region in 28nm bulk NMOSFETs. Solid-State Electronics, 2017, 128, 31-36.	1.4	3
49	A Self-contained Defect-aware Module for Realistic Simulations of LFN, RTN and Time-dependent Variability in FD-SOI Devices and Circuits. , 2018, , .		3
50	Influence of AC signal oscillator level on effective mobility measurement by split Câ€“V technique in MOSFETs. Electronics Letters, 2016, 52, 1492-1493.	1.0	2
51	Impact of Inter-Tier Coupling on Static and Noise Performance in 3D Sequential Integration Technology. , 2019, , .		2
52	Inter-tier electrostatic coupling effects in 3D sequential integration devices and circuits. Solid-State Electronics, 2020, 168, 107715.	1.4	2
53	VERILOR: A Verilog-A Model of Lorentzian Spectra for Simulating Trap-related Noise in CMOS Circuits. , 2021, , .		2
54	Hot carrier degradation mechanisms of short-channel FDSOI n-MOSFETs. , 2015, , .		1

#	Article	IF	Citations
55	Charge Pumping in Ultrathin SOI Tunnel FETs: Impact of Back-Gate Voltage. ECS Transactions, 2019, 89, 111-120.	0.5	1
56	Influence of series resistance on the experimental extraction of FinFET noise parameters. , 2020, , .		1
57	â€œPinch to Detectâ€• A Method to Increase the Number of Detectable RTN Traps in Nano-scale MOSFETs. , 2021, , .		1
58	Parasitic Coupling in 3D Sequential Integration: The Example of a Two-Layer 3D Pixel. Technologies, 2022, 10, 38.	5.1	1
59	Full front and back gate voltage range method for the parameter extraction of advanced FDSOI CMOS devices. , 2015, , .		0
60	Statistical low-frequency noise characterization in sub-15 nm Si/SiGe nanowire Trigate pMOSFETs. , 2017, , .		0
61	Impact of Low-Temperature Coolcubeâ„¢ Process on the Performance of FDSOI Tunnel FETs. , 2018, , .		0
62	1/f Noise Characterization of Piezoresistive Nano-Gauges for MEMS Sensors. , 2018, , .		0
63	Low-frequency noise in surface-treated AlGaN/GaN HFETs. , 2018, , .		0