Fadi J Kurdahi

List of Publications by Year in Descending Order

125 papers	990 citations	16 h-index	24 g-index
150 ext. papers	1,292 ext. citations	3.1 avg, IF	4.45 L-index

#	Paper	IF	Citations
125	In-memory Associative Processors: Tutorial, Potential, and Challenges. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	2
124	Textile-integrated metamaterials for near-field multibody area networks. *Nature Electronics*, **2021**, 4, 808-817	28.4	14
123	Predicting Failures in Embedded Systems Using Long Short-Term Inference. *IEEE Embedded Systems Letters*, **2021**, 13, 85-89	1	
122	Design Exploration of Sensing Techniques in 2T-2R Resistive Ternary CAMs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 762-766	3.5	5
121	CFFNN: Cross Feature Fusion Neural Network for Collaborative Filtering. *IEEE Transactions on Knowledge and Data Engineering*, **2021**, 1-1	4.2	10
120	NEWERTRACK: ML-Based Accurate Tracking of In-Mouth Nutrient Sensors Position Using Spectrum-Wide Information. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3833-3841	2.5	5
119	Error-triggered Three-Factor Learning Dynamics for Crossbar Arrays **2020**,		8
118	Spiking neural networks for inference and learning: a memristor-based design perspective **2020**, 499-530		3
117	IR-QNN Framework: An IR Drop-Aware Offline Training of Quantized Crossbar Arrays. *IEEE Access*, **2020**, 8, 228392-228408	3.5	7
116	Are CNNs Reliable Enough for Critical Applications? An Exploratory Study. *IEEE Design and Test*, **2020**, 37, 76-83	1.4	9
115	Learning to Predict IR Drop with Effective Training for ReRAM-based Neural Network Hardware **2020**,		6
114	The Self-Aware Information Processing Factory Paradigm for Mixed-Critical Multiprocessing. *IEEE Transactions on Emerging Topics in Computing*, **2020**, 1-1	4.1	1
113	On-Chip Error-Triggered Learning of Multi-Layer Memristive Spiking Neural Networks. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2020**, 10, 522-535	5.2	6
112	Power Performance Tradeoffs Using Adaptive Bit Width Adjustments on Resistive Associative Processors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 302-312	3.9	5
111	IBCFAP: Intra-Body Communications Five-Layers Arm Phantom Model. *IEEE Access*, **2019**, 7, 93701-93710	3.5	1
110	An Ultra-Area-Efficient 1024-Point In-Memory FFT Processor. *Micromachines*, **2019**, 10,	3.3	5
109	Mask Technique for Fast and Efficient Training of Binary Resistive Crossbar Arrays. *IEEE Nanotechnology Magazine*, **2019**, 18, 704-716	2.6	13

108	Efficient Tracing Methodology Using Automata Processor. *Transactions on Embedded Computing Systems*, **2019**, 18, 1-18	1.8	4
107	Sensitivity of Galvanic Intra-Body Communication Channel to System Parameters. *Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering*, **2019**, 150-160	0.2	
106	Non-Stationary Polar Codes for Resistive Memories **2019**,		4
105	The information processing factory **2019**,		3
104	Independent Component Analysis Using RRAMs. *IEEE Nanotechnology Magazine*, **2019**, 18, 611-615	2.6	11
103	A Two-Dimensional Associative Processor. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 1659-1670	2.6	7
102	Rapid in-memory matrix multiplication using associative processor **2018**,		5
101	Modeling and Analysis of Passive Switching Crossbar Arrays. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 270-282	3.9	30
100	Physical Multi-Layer Phantoms for Intra-Body Communications. *IEEE Access*, **2018**, 6, 42812-42821	3.5	6
99	Power optimization techniques for associative processors. *Journal of Systems Architecture*, **2018**, 90, 44-53	5.5	3
98	Platform-Centric Self-Awareness as a Key Enabler for Controlling Changes in CPS. *Proceedings of the IEEE*, **2018**, 106, 1543-1567	14.3	11
97	Design methodologies for enabling self-awareness in autonomous systems **2018**,		6
96	A Hybrid Approximate Computing Approach for Associative In-Memory Processors. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2018**, 8, 758-769	5.2	11
95	AS8-static random access memory (SRAM): asymmetric SRAM architecture for soft error hardening enhancement. *IET Circuits, Devices and Systems*, **2017**, 11, 89-94	1.1	22
94	Reliability Enhancement of Low-Power Sequential Circuits Using Reconfigurable Pulsed Latches. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 1803-1814	3.9	6
93	Approximate Memristive In-memory Computing. *Transactions on Embedded Computing Systems*, **2017**, 16, 1-18	1.8	15
92	Efficient pulsed-latch implementation for multiport register files **2017**,		2
91	Low Latency Approximate Adder for Highly Correlated Input Streams **2017**,		1

90	On one step row readout technique of selector-less resistive arrays **2017**,		3
89	On the Optimum Data Carrier for Intra-body Communication Applications **2017**,		2
88	Microarchitecture-Level SoC Design **2017**, 867-913		
87	Conquering MPSoC complexity with principles of a self-aware information processing factory **2016**,		5
86	Microarchitecture-Level SoC Design **2016**, 1-46		
85	Process variations-aware resistive associative processor design **2016**,		4
84	A System-Level Exploration of Power Delivery Architectures for Near-Threshold Manycores Considering Performance Constraints **2016**,		2
83	Thermal sensor allocation for SoCs based on temperature gradients **2015**,		3
82	DWT-based watermarking technique for video authentication **2015**,		3
81	Intra-body communication model based on variable biological parameters **2015**,		6
80	NUVA: Architectural support for runtime verification of parametric specifications over multicores **2015**,		9
79	. *IEEE Embedded Systems Letters*, **2015**, 7, 37-40	1	4
78	Equi-Noise: A Statistical Model That Combines Embedded Memory Failures and Channel Noise. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 407-419	3.9	6
77	. *IEEE Transactions on Circuits and Systems for Video Technology*, **2014**, 24, 1594-1604	6.4	1
76	Joint Power Management and Adaptive Modulation and Coding for Wireless Communications Systems With Unreliable Buffering Memories. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 2456-2465	3.9	3
75	Memristor Multiport Readout: A Closed-Form Solution for Sneak Paths. *IEEE Nanotechnology Magazine*, **2014**, 13, 274-282	2.6	60
74	Multicopy Cache. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-27	1.8	2
73	State dependent statistical timing model for voltage scaled circuits **2014**,		3

72	Algorithms and Architectures of Energy-Efficient Error-Resilient MIMO Detectors for Memory-Dominated Wireless Communication Systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 2159-2171	3.9	6
71	A survey of cross-layer power-reliability tradeoffs in multi and many core systems-on-chip. *Microprocessors and Microsystems*, **2013**, 37, 760-771	2.4	4
70	Heterogeneous memory management for 3D-DRAM and external DRAM with QoS **2013**,		3
69	Fast error aware model for arithmetic and logic circuits **2012**,		14
68	Parity-based mono-Copy Cache for low power consumption and high reliability **2012**,		3
67	Error resilient MIMO detector for memory-dominated wireless communication systems **2012**,		3
66	Variation Trained Drowsy Cache (VTD-Cache): A History Trained Variation Aware Drowsy Cache for Fine Grain Voltage Scaling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 630-642	2.6	7
65	Error-Aware Algorithm/Architecture Coexploration for Video Over Wireless Applications. *Transactions on Embedded Computing Systems*, **2012**, 11S, 1-23	1.8	4
64	Reconfigurable filter implementation of a matched-filter based spectrum sensor for Cognitive Radio systems **2011**,		6
63	A Multi-Granularity Power Modeling Methodology for Embedded Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 668-681	2.6	16
62	Embedded Memories Fault-Tolerant Pre- and Post-Silicon Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1916-1921	2.6	5
61	Adjustable supply voltages and refresh cycle for process variations, temperature changes, and device degradation adaptation in 1T1C embedded DRAM **2011**,		1
60	On leakage power optimization in clock tree networks for ASICs and general-purpose processors. *Sustainable Computing: Informatics and Systems*, **2011**, 1, 75-87	3	3
59	Reliability-aware placement in SRAM-based FPGA for voltage scaling realization in the presence of process variations **2011**,		1
58	Area, reconfiguration delay and reliability trade-offs in designing reliable multi-mode FIR filters **2011**,		1
57	A Class of Low Power Error Compensation Iterative Decoders **2011**,		9
56	Adjustable supply voltages and refresh cycle for process variations and temperature changing adaptation in DRAM to minimize power consumption **2011**,		1
55	Inquisitive Defect Cache: A Means of Combating Manufacturing Induced Process Variation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1597-1609	2.6	17

54	FFT processing through faulty memories in OFDM based systems **2010**,		3
53	Placement-aware partial reconfiguration for a class of FIR-like structures **2010**,		1
52	A combined channel and hardware noise resilient Viterbi decoder **2010**,		18
51	A Unified Hardware and Channel Noise Model for Communication Systems **2010**,		10
50	CAPPS: A Framework for Power-Performance Tradeoffs in Bus-Matrix-Based On-Chip Communication Architecture Synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 209-221	2.6	6
49	Low-Power Multimedia System Design by Aggressive Voltage Scaling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 852-856	2.6	30
48	Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1376-1380	2.6	11
47	Post-synthesis sleep transistor insertion for leakage power optimization in clock tree networks **2010**,		2
46	Process variation aware transcoding for low power H.264 decoding **2010**,		3
45	E 2010,		26
44	RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor. *Lecture Notes in Computer Science*, **2010**, 216-231	0.9	7
43	TRAM: A tool for Temperature and Reliability Aware Memory Design **2009**,		2
42	A Low Power JPEG2000 Encoder With Iterative and Fault Tolerant Error Concealment. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 827-837	2.6	14
41	System-level PVT variation-aware power exploration of on-chip communication architectures. *ACM Transactions on Design Automation of Electronic Systems*, **2009**, 14, 1-25	1.5	1
40	Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications **2009** ,		2
39	Size-Reconfiguration Delay Tradeoffs for a Class of DSP Blocks in Multi-mode Communication Systems **2009**,		6
38	On chip Communication-Architecture Based Thermal Management for SoCs **2009**,		1
37	A fault tolerant cache architecture for sub 500mV operation **2009**,		24

36	Thermal Aware Global Routing of VLSI Chips for Enhanced Reliability **2008**,		7
35	System level performance analysis of carbon nanotube global interconnects for emerging chip multiprocessors **2008**,		6
34	A partial memory protection scheme for higher effective yield of embedded memory for video data **2008**,		1
33	Incorporating PVT Variations in System-Level Power Exploration of On-Chip Communication Architectures **2008**,		2
32	Cross-layer co-exploration of exploiting error resilience for video over wireless applications **2008**,		5
31	Methodology for multi-granularity embedded processor power model generation for an ESL design flow **2008**,		6
30	STEFAL: A System Level Temperature- and Floorplan-Aware Leakage Power Estimator for SoCs **2007**,		6
29	Error-Aware Design **2007**,		8
28	Limits on voltage scaling for caches utilizing fault tolerant techniques **2007**,		8
27	Exploiting Fault Tolerance Towards Power Efficient Wireless Multimedia Applications **2007**,		3
26	Cross Layer Error Exploitation for Aggressive Voltage Scaling **2007**,		26
25	A scalable embedded JPEG 2000 architecture. *Journal of Systems Architecture*, **2007**, 53, 524-538	5.5	5
24	Reducing Off-Chip Memory Access via Stream-Conscious Tiling on Multimedia Applications. *International Journal of Parallel Programming*, **2007**, 35, 63-98	1.5	0
23	A hierarchical pipelining architecture and FPGA implementation for lifting-based 2-D DWT. *Journal of Real-Time Image Processing*, **2007**, 2, 281-291	1.9	2
22	Power Management for Cognitive Radio Platforms **2007**,		7
21	LEAF: A System Level Leakage-Aware Floorplanner for SoCs **2007**,		14
20	Fault Tolerant Approaches Targeting Ultra Low Power Communications System Design. *IEEE Vehicular Technology Conference*, **2007**,	0.1	4
19	System level power estimation methodology with H.264 decoder prediction IP case study **2007**,		8

18	A Coarse-Grain Dynamically Reconfigurable System and Compilation Framework **2007**, 181-215		1
17	Floorplan driven leakage power aware IP-based SoC design space exploration **2006**,		3
16	System-level power-performance trade-offs in bus matrix communication architecture synthesis **2006**,		21
15	Compile-time area estimation for LUT-based FPGAs. *ACM Transactions on Design Automation of Electronic Systems*, **2006**, 11, 104-122	1.5	21
14	**2006**,		7
13	Design and Analysis of Low Power Image Filters Toward Defect-Resilient Embedded Memories for Multimedia SoCs. *Lecture Notes in Computer Science*, **2006**, 295-308	0.9	4
12	Improving effective yield through error tolerant system design **2005**,		8
11	Automatic compilation to a coarse-grained reconfigurable system-opn-chip. *Transactions on Embedded Computing Systems*, **2003**, 2, 560-589	1.8	23
10	A case study of mapping a software-defined radio (SDR) application on a reconfigurable DSP core **2003**,		4
9	Kernel scheduling techniques for efficient solution space exploration in reconfigurable computing. *Journal of Systems Architecture*, **2001**, 47, 277-292	5.5	6
8	A compiler framework for mapping applications to a coarse-grained reconfigurable computer architecture **2001**,		31
7	Design and Implementation of the MorphoSys Reconfigurable Computing Processor. *Journal of Signal Processing Systems*, **2000**, 24, 147-164		46
6	MorphoSys **2000**,		32
5	System-level Time-stationary Control Synthesis for Pipelined Data Paths. *VLSI Design*, **1999**, 9, 159-180		
4	MorphoSys: a reconfigurable processor targeted to high performance image application. *Lecture Notes in Computer Science*, **1999**, 661-669	0.9	1
3	Kernel scheduling in reconfigurable computing **1999**,		6
2	The MorphoSys Parallel Reconfigurable System. *Lecture Notes in Computer Science*, **1999**, 727-734	0.9	13
1	Register-Transfer Synthesis of Pipelined Data Paths. *VLSI Design*, **1994**, 2, 17-32		0