Seung-Tak Ryu

List of Publications by Year
in descending order

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63 papers	1,651 citations	304743 22 h-index	289244 40 g-index
63 all docs	63 docs citations	63 times ranked	1875 citing authors

#	Article	IF	Citations
1	A 7-Bit Two-Step Flash ADC With Sample-and-Hold Sharing Technique. IEEE Journal of Solid-State Circuits, 2022, 57, 2791-2801.	5.4	10
2	A 4th-Order Continuous-Time Delta-Sigma Modulator With Hybrid Noise-Coupling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3635-3639.	3.0	4
3	MixedNet: Network Design Strategies for Cost-Effective Quantized CNNs. IEEE Access, 2021, 9, 117554-117564.	4.2	0
4	An 8-Bit 1-GS/s Asynchronous Loop-Unrolled SAR-Flash ADC With Complementary Dynamic Amplifiers in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 1216-1226.	5.4	16
5	A 28-nm 10-b 2.2-GS/s 18.2-mW Relative-Prime Time-Interleaved Sub-Ranging SAR ADC With On-Chip Background Skew Calibration. IEEE Journal of Solid-State Circuits, 2021, 56, 2691-2700.	5.4	10
6	A 4th-order CT I-DSM with Digital Noise Coupling and Input Pre-conversion Method for Initialization. , 2021, , .		3
7	A 40-nm CMOS 7-b 32-GS/s SAR ADC With Background Channel Mismatch Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 610-614.	3.0	9
8	Air-Gap-Insensitive IPT Pad With Ferromagnetic and Conductive Plates. IEEE Transactions on Power Electronics, 2020, 35, 7863-7872.	7.9	21
9	A Single-Supply CDAC-Based Buffer-Embedding SAR ADC With Skip-Reset Scheme Having Inherent Chopping Capability. IEEE Journal of Solid-State Circuits, 2020, 55, 2660-2669.	5.4	9
10	Compact Mixed-Signal Convolutional Neural Network Using a Single Modular Neuron. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 5189-5199.	5.4	1
11	Recycling of Particulate Photoabsorbers for Highly Stable Solar Desalination Operation. ACS Applied Energy Materials, 2020, 3, 8295-8301.	5.1	9
12	A 28-nm CMOS 12-Bit 250-MS/s Voltage-Current-Time Domain 3-Stage Pipelined ADC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2843-2847.	3.0	9
13	A 40-nm CMOS 12b 120-MS/s Nonbinary SAR-Assisted SAR ADC With Double Clock-Rate Coarse Decision. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2833-2837.	3.0	15
14	A 9.1-ENOB 6-mW 10-Bit 500-MS/s Pipelined-SAR ADC With Current-Mode Residue Processing in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 2532-2542.	5.4	13
15	Three-dimensional solar steam generation device with additional non-photothermal evaporation. Desalination, 2019, 469, 114091.	8.2	31
16	A Reference-Free Temperature-Dependency-Compensating Readout Scheme for Phase-Change Memory Using Flash-ADC-Configured Sense Amplifiers. IEEE Journal of Solid-State Circuits, 2019, 54, 1812-1823.	5.4	4
17	Noise analysis of replica driving technique and its verification to 12â€bit 200â€…MS/s pipelined ADC. IET Circuits, Devices and Systems, 2019, 13, 1277-1283.	1.4	0
18	New Curved Reflectors for Significantly Enhanced Solar Power Generation in Four Seasons. Energies, 2019, 12, 4602.	3.1	6

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19	A 65-nm CMOS 6-bit 2.5-GS/s 7.5-mW 8<inline-formula> <tex-math notation="LaTeX">$imes$ </tex-math> </inline-formula> Time-Domain Interpolating Flash ADC With Sequential Slope-Matching Offset Calibration. IEEE Journal of Solid-State Circuits, 2019, 54, 288-297.	5.4	27
20	A Single-Supply Buffer-Embedding SAR ADC with Skip-Reset having Inherent Chopping Capability. , 2019, , .		5
21	A 2.7-M Pixels 64-mW CMOS Image Sensor With Multicolumn-Parallel Noise-Shaping SAR ADCs. IEEE Transactions on Electron Devices, 2018, 65, 1119-1126.	3.0	17
22	A 65-nm CMOS 6-Bit 20 GS/s Time-Interleaved DAC With Full-Binary Sub-DACs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1154-1158.	3.0	9
23	A Reusable Code-Based SAR ADC Design With CDAC Compiler and Synthesizable Analog Building Blocks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1904-1908.	3.0	29
24	A 4.2-mW 10-MHz BW 74.4-dB SNDR Continuous-Time Delta-Sigma Modulator With SAR-Assisted Digital-Domain Noise Coupling. IEEE Journal of Solid-State Circuits, 2018, 53, 1139-1148.	5.4	22
25	A 65 nm 0.08-to-680 MHz Low-Power Synthesizable MDLL With Nested-Delay Cell and Background Static Phase Offset Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 281-285.	3.0	6
26	Introduction to the Special Section on the 2017 Asian Solid-State Circuits Conference (A-SSCC). IEEE Journal of Solid-State Circuits, 2018, 53, 2739-2740.	5.4	0
27	A Time-Interleaved 12-b 270-MS/s SAR ADC With Virtual-Timing-Reference Timing-Skew Calibration Scheme. IEEE Journal of Solid-State Circuits, 2018, 53, 2584-2594.	5.4	23
28	A 18.5 nW 12-bit 1-kS/s Reset-Energy Saving SAR ADC for Bio-Signal Acquisition in 0.18-Î¼m CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, , 1-11.	5.4	5
29	Normalized-Full-Scale-Referencing Digital-Domain Linearity Calibration for SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 322-332.	5.4	17
30	A Dual-Imaging Speed-Enhanced CMOS Image Sensor for Real-Time Edge Image Extraction. IEEE Journal of Solid-State Circuits, 2017, 52, 2488-2497.	5.4	14
31	Fully flexible, lightweight, high performance all-solid-state supercapacitor based on 3-Dimensional-graphene/graphite-paper. Journal of Power Sources, 2017, 337, 159-165.	7.8	250
32	An incremental zoom sturdy MASH ADC. , 2017, , .		2
33	Introduction to the Special Issue on the 2017 IEEE International Solid-State Circuits Conference. IEEE Journal of Solid-State Circuits, 2017, 52, 3115-3118.	5.4	0
34	A 54-Î¼W fast-settling arterial pulse wave sensor for wrist watch type system. , 2016, , .		1
35	Realization of high performance flexible wire supercapacitors based on 3-dimensional NiCo₂O₄/Ni fibers. Journal of Materials Chemistry A, 2016, 4, 4718-4727.	10.3	100
36	A Delta-Readout Scheme for Low-Power CMOS Image Sensors With Multi-Column-Parallel SAR ADCs. IEEE Journal of Solid-State Circuits, 2016, 51, 2262-2273.	5.4	47

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37	A 0.6 V 12 b 10 MS/s Low-Noise Asynchronous SAR-Assisted Time-Interleaved SAR (SATI-SAR) ADC. IEEE Journal of Solid-State Circuits, 2016, 51, 1826-1839.	5.4	65
38	A Low-Power TDC-Configured Logarithmic Resistance Sensor for MLC PCM Readout. IEEE Sensors Journal, 2016, 16, 5524-5535.	4.7	8
39	A Sign-Equality-Based Background Timing-Mismatch Calibration Algorithm for Time-Interleaved ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 518-522.	3.0	23
40	A SUC-Based Full-Binary 6-bit 3.1-GS/s 17.7-mW Current-Steering DAC in 0.038 mm^{2}. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 794-798.	3.1	17
41	Ternary-level thermometer C-DAC switching scheme for flash-assisted SAR ADCs. IEICE Electronics Express, 2015, 12, 20150302-20150302.	0.8	1
42	A Decision-Error-Tolerant 45 nm CMOS 7b 1 GS/s Nonbinary 2b/Cycle SAR ADC. IEEE Journal of Solid-State Circuits, 2015, 50, 543-555.	5.4	79
43	A 15 Âµm-Pitch, 8.7-ENOB, 13-Mcells/sec Logarithmic Readout Circuit for Multi-Level Cell Phase Change Memory. IEEE Journal of Solid-State Circuits, 2015, 50, 2431-2440.	5.4	7
44	A 65 nm CMOS 7b 2 GS/s 20.7 mW Flash ADC With Cascaded Latch Interpolation. IEEE Journal of Solid-State Circuits, 2015, 50, 2319-2330.	5.4	40
45	A dual channel 10-b pipelined ADC for Intelligent Transport System. , 2014, , .		1
46	38.1: A Lowâ€Power Fast Readout Circuit using a Dualâ€Mode Sensing Algorithm for Mediumâ€Size Capacitive Touch Screen Panels. Digest of Technical Papers SID International Symposium, 2014, 45, 540-543.	0.3	3
47	A 10-Bit Column-Driver IC With Parasitic-Insensitive Iterative Charge-Sharing Based Capacitor-String Interpolation for Mobile Active-Matrix LCDs. IEEE Journal of Solid-State Circuits, 2014, 49, 766-782.	5.4	32
48	A 10-Bit 40-MS/s Pipelined ADC With a Wide Range Operating Temperature for WAVE Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 6-10.	3.0	10
49	An 88-dB Max-SFDR 12-bit SAR ADC With Speed-Enhanced ADEC and Dual Registers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 562-566.	3.0	14
50	A Noise-Immune High-Speed Readout Circuit for In-Cell Touch Screen Panels. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1800-1809.	5.4	28
51	An Asynchronous Sampling-Based 128 $imes$ 128 Direct Photon-Counting X-Ray Image Detector with Multi-Energy Discrimination and High Spatial Resolution. IEEE Journal of Solid-State Circuits, 2013, 48, 541-558.	5.4	23
52	A Replica-Driving Technique for High Performance SC Circuits and Pipelined ADC Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 557-561.	3.0	15
53	A 6-b 4.1-GS/s Flash ADC With Time-Domain Latch Interpolation in 90-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 1429-1441.	5.4	49
54	A Precise Decibel-Linear Programmable Gain Amplifier Using a Constant Current-Density Function. IEEE Transactions on Microwave Theory and Techniques, 2012, 60, 2843-2850.	4.6	47

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55	A Two-Channel Asynchronous SAR ADC With Metastable-Then-Set Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 765-769.	3.1	20
56	A 40 mV Transformer-Reuse Self-Startup Boost Converter With MPPT Control for Thermoelectric Energy Harvesting. IEEE Journal of Solid-State Circuits, 2012, 47, 3055-3067.	5.4	175
57	A Long Reset-Time Power-On Reset Circuit With Brown-Out Detection Capability. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 778-782.	3.0	35
58	A 550-$muhbox{W}$ 10-b 40-MS/s SAR ADC With Multistep Addition-Only Digital Error Correction. IEEE Journal of Solid-State Circuits, 2011, 46, 1881-1892.	5.4	94
59	A Compact-Sized 9-Bit Switched-Current DAC for AMOLED Mobile Display Drivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 887-891.	3.0	8
60	6.1: A Size Efficient 10b DAC with Multi-path Current Interpolation and Weighted Tranconductors for the AMLCD Displays. Digest of Technical Papers SID International Symposium, 2010, 41, 54.	0.3	1
61	A regulator-free 84dB DR audio-band ADC for compact digital microphones. , 2010, , .		2
62	A 10-bit 50-MS/s Pipelined ADC With Opamp Current Reuse. IEEE Journal of Solid-State Circuits, 2007, 42, 475-485.	5.4	70
63	A 14-b linear capacitor self-trimming pipelined ADC. IEEE Journal of Solid-State Circuits, 2004, 39, 2046-2051.	5.4	40