Shanthi Pavan

List of Publications by Year
in descending order

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77 papers	1,646 citations	279798 23 h-index	302126 39 g-index
77 all docs	77 docs citations	77 times ranked	747 citing authors

#	Article	IF	Citations
1	Alias Rejection in CT Delta-Sigma ADCs Using Virtual-Ground-Switched Resistor Feedback. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1991-1995.	3.0	0
2	Analysis of RC Time-Constant Variations in Continuous-Time Pipelined ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 530-540.	5.4	4
3	Systematic Development of CMOS Fixed-Transconductance Bias Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2394-2397.	3.0	2
4	A 0.37mm² 250kHz-BW 95dB-SNDR CTDSM with Low-Cost 2nd-order Vector-Quantizer DEM. , 2022, , .		3
5	Improved Multistage Continuous-Time Pipelined Analog-to-Digital Converters and the Implicit Decimation Property. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3102-3113.	5.4	5
6	Design of High-Resolution Continuous-Time Deltaâ€“Sigma Data Converters With Dual Return-to-Open DACs. IEEE Journal of Solid-State Circuits, 2022, 57, 3418-3428.	5.4	5
7	Analysis and Design of a 20-MHz Bandwidth Continuous-Time Delta-Sigma Modulator With Time-Interleaved Virtual-Ground-Switched FIR Feedback. IEEE Journal of Solid-State Circuits, 2021, 56, 729-738.	5.4	17
8	A 65-nm CMOS Continuous-Time Pipeline ADC Achieving 70-dB SNDR in 100-MHz Bandwidth. IEEE Solid-State Circuits Letters, 2021, 4, 92-95.	2.0	13
9	Continuous-Time Pipelined Analog-to-Digital Converters: A Mini-Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 810-815.	3.0	18
10	Continuous-Time Incremental Delta-Sigma Modulators With FIR Feedback. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3222-3231.	5.4	3
11	Improved Continuous-Time Delta-Sigma Modulators With Embedded Active Filtering. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3778-3789.	5.4	5
12	Design Techniques for High-Resolution Continuous-Time Deltaâ€“Sigma Converters With Low In-Band Noise Spectral Density. IEEE Journal of Solid-State Circuits, 2020, 55, 2429-2442.	5.4	15
13	16.6 An 800MHz-BW VCO-Based Continuous-Time Pipelined ADC with Inherent Anti-Aliasing and On-Chip Digital Reconstruction Filter. , 2020, , .		27
14	Continuous-Time Delta-Sigma Converters with Finite-Impulse-Response (FIR) Feedback. , 2020, , 77-90.		0
15	Analysis and Design of an Audio Continuous-Time 1-X FIR-MASH Deltaâ€“Sigma Modulator. IEEE Journal of Solid-State Circuits, 2020, 55, 2649-2659.	5.4	16
16	Analysis and Design of a Multi-Step Bias-Flip Rectifier for Piezoelectric Energy Harvesting. IEEE Journal of Solid-State Circuits, 2019, 54, 2590-2600.	5.4	30
17	Improved Offline Calibration of DAC Mismatch Errors in Deltaâ€“Sigma Data Converters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1618-1622.	3.0	7
18	Degradation of Alias Rejection in Continuous-Time Bandpass Delta-Sigma Converters due to Weak Loop Filter Nonlinearities. , 2019, , .		0

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19	Analysis and Design of Cyclic Switched-Capacitor DCâ€“DC Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3227-3237.	5.4	8
20	Unified Analysis, Modeling, and Simulation of Chopping Artifacts in Continuous-Time Delta-Sigma Modulators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2831-2842.	5.4	10
21	An Alternative Approach to Bodeâ€™s Noise Theorem. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 738-742.	3.0	2
22	A 265Î¼W Continuous-Time 1â€“2 MASH ADC Achieving 100.6 dB SNDR in a 24 kHz Bandwidth. , 2019, , .		0
23	Generalized Analysis of High-Order Switch-RC <inline-formula> <tex-math notation="LaTeX">N </tex-math> </inline-formula>-Path Mixers/Filters Using the Adjoint Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3267-3278.	5.4	16
24	What Architecture Should I Choose for my Continuous-Time Delta-Sigma Modulator?. , 2018, , .		0
25	Improved Chopping in Continuous-Time Deltaâ€“Sigma Converters Using FIR Feedback and <inline-formula> <tex-math notation="LaTeX">${N}$ </tex-math> </inline-formula>-Path Techniques. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 552-556.	3.0	2
26	Analysis of the Effect of Source Capacitance and Inductance on N -Path Mixers and Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1469-1480.	5.4	34
27	Continuous-Time Delta-Sigma Modulators With Time-Interleaved FIR Feedback. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 434-443.	5.4	18
28	Multi-Step Bias-Flip Rectification for Piezoelectric Energy Harvesting. , 2018, , .		5
29	Practical design and simulation techniques for continuous-time Î”Î£ converters. , 2018, , .		0
30	Finite-impulse-response (FIR) feedback in continuous-time delta-sigma converters. , 2018, , .		5
31	Degradation of Alias Rejection in Continuous-Time Deltaâ€“Sigma Modulators by Weak Loop-Filter Nonlinearities. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3207-3215.	5.4	2
32	Design and Analysis of an 8 mW, 1 GHz Span, Passive Spectrum Scanner With >+31 dBm Out-of-Band IIP3 Using Periodically Time-Varying Circuit Components. IEEE Journal of Solid-State Circuits, 2017, 52, 2009-2025.	5.4	11
33	Simplified Unified Analysis of Switched-RC Passive Mixers, Samplers, and N -Path Filters Using the Adjoint Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2714-2725.	5.4	31
34	Analysis of Chopped Integrators, and Its Application to Continuous-Time Delta-Sigma Modulator Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1953-1965.	5.4	21
35	Analysis and Design of Continuous-Time Deltaâ€“Sigma Converters Incorporating Chopping. IEEE Journal of Solid-State Circuits, 2017, 52, 2350-2361.	5.4	68
36	A 9-GS/s 1.125-GHz BW Oversampling Continuous-Time Pipeline ADC Achieving â^’164-dBFS/Hz NSD. IEEE Journal of Solid-State Circuits, 2017, 52, 3219-3234.	5.4	45

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37	Design of Continuous-Time <inline-formula> <tex-math notation="LaTeX">$Delta Sigma $</tex-math> </inline-formula> Modulators With Dual Switched-Capacitor Return-to-Zero DACs. IEEE Journal of Solid-State Circuits, 2016, 51, 1619-1629.	5.4	13
38	Guest Editorial: Next-Generation Delta-Sigma Converters. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 481-483.	3.6	0
39	Outgoing Editorial. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2793-2794.	5.4	0
40	Next-Generation Delta-Sigma Converters: Trends and Perspectives. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 484-499.	3.6	64
41	Characterization Techniques for High Speed Oversampled Data Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1313-1320.	5.4	5
42	Continuous-Time Delta-Sigma Modulator Design Using the Method of Moments. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1629-1637.	5.4	34
43	Interreciprocity in Linear Periodically Time-Varying Networks With Sampled Outputs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 686-690.	3.0	18
44	Design Techniques for Continuous-Time Î”Î£ Modulators With Embedded Active Filtering. IEEE Journal of Solid-State Circuits, 2014, 49, 2187-2198.	5.4	39
45	Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback. IEEE Journal of Solid-State Circuits, 2014, 49, 2515-2525.	5.4	96
46	Design of Lumped-Component Programmable Delay Elements for Ultra-Wideband Beamforming. IEEE Journal of Solid-State Circuits, 2014, 49, 1800-1814.	5.4	22
47	Simplified Analysis and Simulation of the STF, NTF, and Noise in Continuous-Time <inline-formula> <tex-math notation="TeX">$DeltaSigma$</tex-math></inline-formula> Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 681-685.	3.0	6
48	Continuous-Time <formula formulatype="inline"><tex Notation="TeX">$Delta Sigma $</tex></formula> Modulators With Improved Linearity and Reduced Clock Jitter Sensitivity Using the Switched-Capacitor Return-to-Zero DAC. IEEE Journal of Solid-State Circuits, 2013, 48, 1795-1805.	5.4	27
49	A Time-Domain Perspective of the Signal Transfer Function of a Continuous-Time $DeltaSigma$ Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 81-85.	3.0	2
50	A Miniaturized pH Sensor With an Embedded Counter Electrode and a Readout Circuit. IEEE Sensors Journal, 2013, 13, 1941-1948.	4.7	16
51	A 1.2 V 285μA analog front end chip for a digital hearing aid in 0.13 μm CMOS. , 2013, , .		8
52	A 16 MHz BW 75 dB DR CT $DeltaSigma$ ADC Compensated for More Than One Cycle Excess Loop Delay. IEEE Journal of Solid-State Circuits, 2012, 47, 1884-1895.	5.4	37
53	Device Noise in Continuous-Time Oversampling Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1829-1840.	5.4	5
54	Design Techniques for Wideband Single-Bit Continuous-Time $DeltaSigma$ Modulators With FIR Feedback DACs. IEEE Journal of Solid-State Circuits, 2012, 47, 2865-2879.	5.4	97

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55	Analysis and Design of a High Speed Continuous-time $DeltaSigma$ Modulator Using the Assisted Opamp Technique. IEEE Journal of Solid-State Circuits, 2012, 47, 1615-1625.	5.4	29
56	A 16MHz BW 75dB DR CT ΔΣ ADC compensated for more than one cycle excess loop delay. , 2011, , .		6
57	Active-RC Filters Using the Gm-Assisted OTA-RC Technique. IEEE Journal of Solid-State Circuits, 2011, 46, 1522-1533.	5.4	57
58	Alias Rejection of Continuous-Time $DeltaSigma$ Modulators With Switched-Capacitor Feedback DACs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 233-243.	5.4	47
59	A power efficient continuous time Î”Î£ modulator with 15ÂMHz bandwidth and 70ÂdB dynamic range. Analog Integrated Circuits and Signal Processing, 2010, 63, 397-406.	1.4	3
60	Systematic Design Centering of Continuous Time Oversampling Converters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 158-162.	3.0	58
61	Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique. IEEE Journal of Solid-State Circuits, 2010, 45, 1365-1379.	5.4	71
62	Efficient Simulation of Weak Nonlinearities in Continuous-Time Oversampling Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1925-1934.	5.4	28
63	Widely Programmable High-Frequency Active RC Filters in CMOS Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 327-336.	5.4	54
64	A Power Optimized Continuous-Time $Delta Sigma $ ADC for Audio Applications. IEEE Journal of Solid-State Circuits, 2008, 43, 351-360.	5.4	116
65	Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1119-1123.	3.0	53
66	Accurate Characterization of Integrated Continuous-Time Filters. IEEE Journal of Solid-State Circuits, 2007, 42, 1758-1766.	5.4	11
67	Fundamental Limitations of Continuous-Time Delta–Sigma Modulators Due to Clock Jitter. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 2184-2194.	0.1	81
68	Analysis and Design of Singly Terminated Transmission-Line FIR Adaptive Equalizers. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 401-410.	0.1	7
69	Automatic Tuning of Time Constants in Continuous-Time Delta–Sigma Modulators. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 308-312.	2.2	10
70	Efficient Design Centering of High-Frequency Integrated Continuous-Time Filters. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1481-1488.	0.1	15
71	Analysis of Integrator Nonlinearity in a Class of Continuous-Time Deltaâ€“Sigma Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 1125-1129.	3.0	37
72	A 70-500MHz Programmable CMOS Filter Compensated for MOS Nonquasistatic Effects. , 2006, , .		11

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73	Rapid Simulation of Current Steering Digital-to-Analog Converters using Verilog-A. , 2006, , .		1
74	A Technique for Accurate Frequency Response Measurement of Integrated Continuous-Time Filters. , 2006, , .		3
75	DESIGN CONSIDERATIONS FOR INTEGRATED MODULATOR DRIVERS IN SILICON GERMANIUM TECHNOLOGY. International Journal of High Speed Electronics and Systems, 2005, 15, 477-495.	0.7	1
76	A fixed transconductance bias technique for CMOS analog integrated circuits. , 0, , .		7
77	Transmission Line based FIR Structures for High Speed Adaptive Equalization. , 0, , .		3