Marco Platzner

List of Publications by Year
in descending order

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142	1,610	687363	501196
papers	citations	13	28
		h-index	g-index

150	150	150	972
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Exploiting Hardware-Based Data-Parallel and Multithreading Models for Smart Edge Computing in Reconfigurable FPGAs. IEEE Transactions on Computers, 2022, 71, 2903-2914.	3.4	1
2	Design of Distributed Reconfigurable Robotics Systems with ReconROS. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-20.	2.5	4
3	MUSCAT: MUS-based Circuit Approximation Technique. , 2022, , .		4
4	Timing Optimization for Virtual FPGA Configurations. Lecture Notes in Computer Science, 2021, , 50-64.	1.3	0
5	Immersive augmented reality system for the training of pattern classification control with a myoelectric prosthesis. Journal of NeuroEngineering and Rehabilitation, 2021, 18, 25.	4.6	21
6	LDAX. , 2021, , .		1
7	MCTS-based Synthesis Towards Efficient Approximate Accelerators. , 2021, , .		1
8	Optimization of Application-Specific L1 Cache Translation Functions of the LEON3 Processor. Advances in Intelligent Systems and Computing, 2021, , 266-276.	0.6	1
9	Software/Hardware Co-Verification for Custom Instruction Set Processors. IEEE Access, 2021, 9, 160559-160579.	4.2	2
10	Evolution of application-specific cache mappings. International Journal of Hybrid Intelligent Systems, 2020, 16, 149-161.	1.2	0
11	Proof-Carrying Approximate Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2084-2088.	3.1	0
12	Dynamic Reliability Management for FPGA-Based Systems. International Journal of Reconfigurable Computing, 2020, 2020, 1-19.	0.2	4
13	DeepWind: An Accurate Wind Turbine Condition Monitoring Framework via Deep Learning on Embedded Platforms. , 2020, , .		8
14	MigHEFT: DAG-based Scheduling of Migratable Tasks on Heterogeneous Compute Nodes. , 2020, , .		1
15	Adaptable Realization of Industrial Analytics Functions on Edge-Devices using Reconfigurable Architectures. Technologien Ful˙r Die Intelligente Automation, 2020, , 73-80.	0.5	1
16	ReconROS: Flexible Hardware Acceleration for ROS2 Applications. , 2020, , .		9
17	A Hybrid Synthesis Methodology for Approximate Circuits. , 2020, , .		1
18	An Approach for Mapping Periodic Real-Time Tasks to Reconfigurable Hardware. , 2019, , .		4

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19	CIRCA: Towards a modular and extensible framework for approximate circuit generation. Microelectronics Reliability, 2019, 99, 277-290.	1.7	15
20	Jump Search. , 2019, , .		8
21	Proof-Carrying Hardware Versus the Stealthy Malicious LUT Hardware Trojan. Lecture Notes in Computer Science, 2019, , 127-136.	1.3	4
22	Zynq-based acceleration of robust high density myoelectric signal processing. Journal of Parallel and Distributed Computing, 2019, 123, 77-89.	4.1	6
23	An Accelerator for Resolution Proof Checking based on FPGA and Hybrid Memory Cube Technology. Journal of Signal Processing Systems, 2019, 91, 1259-1272.	2.1	0
24	Ampehre: An Open Source Measurement Framework for Heterogeneous Compute Nodes. Lecture Notes in Computer Science, 2018, , 73-84.	1.3	2
25	R-Codesign: Codesign Methodology for Real-Time Reconfigurable Embedded Systems Under Energy Constraints. IEEE Access, 2018, 6, 14078-14092.	4.2	23
26	An MCTS-based Framework for Synthesis of Approximate Circuits. , 2018, , .		9
27	A Highly Accurate Energy Model for Task Execution on Heterogeneous Compute Nodes. , 2018, , .		1
28	Combining Local and Global Search: A Multi-objective Evolutionary Algorithm for Cartesian Genetic Programming. Emergence, Complexity and Computation, 2018, , 175-194.	0.3	3
29	An FPGA/HMC-Based Accelerator forÂResolution Proof Checking. Lecture Notes in Computer Science, 2018, , 153-165.	1.3	0
30	A Zynq-based dynamically reconfigurable high density myoelectric prosthesis controller. , 2017, , .		2
31	Evaluating fault-tolerance of redundant FPGA structures using Boolean difference calculus. Microprocessors and Microsystems, 2017, 52, 160-172.	2.8	3
32	Accurate private/shared classification of memory accesses: A run-time analysis system for the LEON3 multi-core processor. , 2017, , .		1
33	Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Computers, 2017, 66, 927-929.	3.4	0
34	The First 25 Years of the FPL Conference. ACM Transactions on Reconfigurable Technology and Systems, 2017, 10, 1-17.	2.5	1
35	reMinMin: A novel static energy-centric list scheduling approach based on real measurements. , 2017, , .		3
36	Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Emerging Topics in Computing, 2017, 5, 207-209.	4.6	1

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37	Proof-Carrying Hardware via Inductive Invariants. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-23.	2.6	4
38	Evaluation methodology for complex non-deterministic functions: A case study in metaheuristic optimization of caches. , 2017, , .		0
39	Computational self-awareness as design approach for visual sensor nodes. , 2017, , .		4
40	Evolvable caches: Optimization of reconfigurable cache mappings for a LEON3/Linux-based multi-core processor. , 2017, , .		0
41	I-Codesign: A Codesign Methodology for Reconfigurable Embedded Systems. Communications in Computer and Information Science, 2017, , 153-174.	0.5	0
42	Adaptive playouts for online learning of policies during Monte Carlo Tree Search. Theoretical Computer Science, 2016, 644, 53-62.	0.9	5
43	Monte-Carlo simulation balancing revisited. , 2016, , .		1
44	Thread shadowing: On the effectiveness of error detection at the hardware thread level. , 2016, , .		1
45	An architecture and design tool flow for embedding a virtual FPGA into a reconfigurable system-on-chip. Computers and Electrical Engineering, 2016, 55, 112-122.	4.8	2
46	Verifying worst-case completion times for reconfigurable hardware modules using proof-carrying hardware. , 2016, , .		1
47	Programming models for reconfigurable manycore systems. , 2016, , .		6
48	Self-aware Computing: Introduction and Motivation. Natural Computing Series, 2016, , 1-5.	2.2	5
49	Self-aware Compute Nodes. Natural Computing Series, 2016, , 145-165.	2.2	1
50	On-the-fly computing. , 2016, , .		2
51	Boolean Difference Based Reliability Evaluation of Fault-Tolerant Circuit Structures on FPGAs. , 2016, , .		0
52	Performance-Centric Scheduling with Task Migration for a Heterogeneous Compute Node in the Data Center. , 2016, , .		8
53	Using Deep Convolutional Neural Networks in Monte Carlo Tree Search. Lecture Notes in Computer Science, 2016, , 11-21.	1.3	3
54	New Co-design Methodology for Real-time Embedded Systems. , 2016, , .		3

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55	ReconOS. , 2016, , 227-244.		1
56	FPGA-based acceleration of high density myoelectric signal processing. , 2015, , .		9
57	Significant papers from the first 25 years of the FPL conference. , 2015, , .		1
58	Comparison of thread signatures for error detection in hybrid multi-cores. , 2015, , .		1
59	Adaptive Playouts in Monte-Carlo Tree Search with Policy-Gradient Reinforcement Learning. Lecture Notes in Computer Science, 2015, , 1-11.	1.3	8
60	Microarchitectural optimization by means of reconfigurable and evolvable cache mappings. , 2015, , .		2
61	Distributed Monte Carlo Tree Search: A Novel Technique and its Application to Computer Go. IEEE Transactions on Games, 2015, 7, 361-374.	1.4	8
62	On-The-Fly Verification of Reconfigurable Image Processing Modules Based on a Proof-Carrying Hardware Approach. Lecture Notes in Computer Science, 2015, , 365-372.	1.3	1
63	Towards self-adaptive caches: A run-time reconfigurable multi-core infrastructure. , 2014, , .		2
64	Analytic reliability evaluation for fault-tolerant circuit structures on FPGAs. , 2014, , .		2
65	Towards robust HD EMG pattern recognition: Reducing electrode displacement effect using structural similarity. , 2014, 2014, 4547-50.		20
66	A hardware/software infrastructure for performance monitoring on LEON3 multicore platforms. , 2014, , .		14
67	Self-Awareness as a Model for Designing and Operating Heterogeneous Multicores. ACM Transactions on Reconfigurable Technology and Systems, 2014, 7, 1-18.	2.5	15
68	FPGA Redundancy Configurations: An Automated Design Space Exploration. , 2014, , .		8
69	Memory security in reconfigurable computers: Combining formal verification with monitoring. , 2014, , .		10
70	Common fate graph patterns in Monte Carlo Tree Search for computer go. , 2014, , .		6
71	Seven recipes for setting your FPGA on fire â€“ A cookbook on heat generators. Microprocessors and Microsystems, 2014, 38, 911-919.	2.8	16
72	An FPGA-Based Reconfigurable Mesh Many-Core. IEEE Transactions on Computers, 2014, 63, 2919-2932.	3.4	10

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73	ReconOS: An Operating System Approach for Reconfigurable Computing. IEEE Micro, 2014, 34, 60-71.	1.8	90
74	Embedding FPGA overlays into configurable Systems-on-Chip: ReconOS meets ZUMA. , 2014, , .		12
75	On Semeai Detection in Monte-Carlo Go. Lecture Notes in Computer Science, 2014, , 14-25.	1.3	2
76	Integrating Software and Hardware Verification. Lecture Notes in Computer Science, 2014, , 307-322.	1.3	2
77	Thread Shadowing: Using Dynamic Redundancy on Hybrid Multi-cores for Error Detection. Lecture Notes in Computer Science, 2014, , 283-290.	1.3	2
78	A self-adaptive heterogeneous multi-core architecture for embedded real-time video object tracking. Journal of Real-Time Image Processing, 2013, 8, 95-110.	3.5	34
79	On-The-Fly Computing: A novel paradigm for individualized IT services. , 2013, , .		14
80	Reducing the limb position effect in pattern recognition based myoelectric control using a high density electrode array. , 2013, , .		12
81	Classification of Electromyographic Signals: Comparing Evolvable Hardware to Conventional Classifiers. IEEE Transactions on Evolutionary Computation, 2013, 17, 46-63.	10.0	17
82	Improving transient state myoelectric signal recognition in hand movement classification using gyroscopes. , 2013, 2013, 6035-8.		4
83	Dynamic reliability management: Reconfiguring reliability-levels of hardware designs at runtime. , 2013, , .		3
84	Reducing classification accuracy degradation of pattern recognition based myoelectric control caused by electrode shift using a high density electrode array. , 2012, 2012, 4324-7.		19
85	Comparison of Bayesian move prediction systems for Computer Go. , 2012, , .		6
86	IMORC: An infrastructure and architecture template for implementing high-performance reconfigurable FPGA accelerators. Microprocessors and Microsystems, 2012, 36, 110-126.	2.8	3
87	Compensating Resource Fluctuations by Means of Evolvable Hardware. International Journal of Adaptive Resilient and Autonomic Systems, 2012, 3, 17-31.	0.3	0
88	Design and architectures for dependable embedded systems. , 2011, , .		73
89	Evolution of Electronic Circuits. Natural Computing Series, 2011, , 125-179.	2.2	10
90	FPGA Acceleration of Communication-Bound Streaming Applications: Architecture Modeling and a 3D Image Compositing Case Study. International Journal of Reconfigurable Computing, 2011, 2011, 1-11.	0.2	1

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91	Performance estimation framework for automated exploration of CPU-accelerator architectures. , 2011, , .		2
92	Memory Virtualization for Multithreaded Reconfigurable Hardware. , 2011, , .		13
93	Achieving hardware security for reconfigurable systems on chip by a proof-carrying code approach. , 2011, , .		12
94	Multithreaded Programming of Reconfigurable Embedded Systems. , 2011, , 31-54.		0
95	Hardware Virtualization on Dynamically Reconfigurable Processors. , 2011, , 82-109.		2
96	Multi-objective Intrinsic Evolution of Embedded Systems. , 2011, , 193-206.		2
97	Proof-Carrying Hardware: Concept and Prototype Tool Flow for Online Verification. International Journal of Reconfigurable Computing, 2010, 2010, 1-11.	0.2	10
98	A Triple Hybrid Interconnect for Many-Cores: Reconfigurable Mesh, NoC and Barrier. , 2010, , .		10
99	Fluctuating emg signals: Investigating long-term effects of pattern matching algorithms. , 2010, 2010, 6357-60.		82
100	A novel hybrid evolutionary strategy and its periodization with multi-objective genetic optimizers. , 2010, , .		5
101	Engineering self-coordinating software intensive systems. , 2010, , .		1
102	Reconfigurable nodes for future networks. , 2010, , .		1
103	ReconOS: An Operating System forÂDynamically Reconfigurable Hardware. , 2010, , 269-290.		6
104	Coping with Resource Fluctuations: The Run-time Reconfigurable Functional Unit Row Classifier Architecture. Lecture Notes in Computer Science, 2010, , 250-261.	1.3	5
105	ARMLang: A language and compiler for programming reconfigurable mesh many-cores. , 2009, , .		7
106	Proof-Carrying Hardware: Towards Runtime Verification of Reconfigurable Modules. , 2009, , .		40
107	Communication Performance Characterization for Reconfigurable Accelerator Design on the XD1000. , 2009, , .		1
108	ReconOS. Transactions on Embedded Computing Systems, 2009, 9, 1-33.	2.9	121

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109	Program-driven fine-grained power management for the reconfigurable mesh. , 2009, , .		0
110	EvoCaches: Application-specific Adaptation of Cache Mappings. , 2009, , .		22
111	An adaptive Sequential Monte Carlo framework with runtime HW/SW repartitioning. , 2009, , .		5
112	IMORC: Application Mapping, Monitoring and Optimization for High-Performance Reconfigurable Computing. , 2009, , .		4
113	Cooperative multithreading in dynamically reconfigurable systems. , 2009, , .		19
114	An accelerator for K-TH nearest neighbor thinning based on the IMORC infrastructure. , 2009, , .		5
115	A Multithreaded Framework for Sequential Monte Carlo Methods on CPU/FPGA Platforms. Lecture Notes in Computer Science, 2009, , 380-385.	1.3	6
116	SPP1148 booth: Fine grain reconfigurable architectures. , 2008, , .		1
117	A portable abstraction layer for hardware threads. , 2008, , .		14
118	Realizing reconfigurable mesh algorithms on softcore arrays. , 2008, , .		4
119	Comparing Evolvable Hardware to Conventional Classifiers for Electromyographic Prosthetic Hand Control. , 2008, , .		17
120	A Comparison of Evolvable Hardware Architectures for Classification Tasks. Lecture Notes in Computer Science, 2008, , 22-33.	1.3	13
121	On Robust Evolution of Digital Hardware. International Federation for Information Processing, 2008, , 213-222.	0.4	4
122	Dynamically Reconfigurable Architectures. Eurasip Journal on Embedded Systems, 2007, 2007, 1-2.	1.2	0
123	Server-based execution of periodic tasks on dynamically reconfigurable hardware. IET Computers and Digital Techniques, 2007, 1, 295.	1.2	5
124	A Many-Core Implementation Based on the Reconfigurable Mesh Model. , 2007, , .		9
125	ReconOS: An RTOS Supporting Hard-and Software Threads. , 2007, , .		50
126	MOVES: A Modular Framework for Hardware Evolution. , 2007, , .		14

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127	Optimal temporal partitioning based on slowdown and retiming. , 2006, , .		1
128	An EDF schedulability test for periodic tasks on reconfigurable hardware devices. ACM SIGPLAN Notices, 2006, 41, 93-102.	0.2	9
129	Executing Hardware Tasks on Dynamically Reconfigurable Devices Under Real-Time Conditions. , 2006, , .		24
130	An EDF schedulability test for periodic tasks on reconfigurable hardware devices. , 2006, , .		24
131	System-level performance evaluation of reconfigurable processors. Microprocessors and Microsystems, 2005, 29, 63-73.	2.8	14
132	Operating systems for reconfigurable embedded platforms: online scheduling of real-time tasks. IEEE Transactions on Computers, 2004, 53, 1393-1407.	3.4	219
133	A Runtime Environment for Reconfigurable Hardware Operating Systems. Lecture Notes in Computer Science, 2004, , 831-835.	1.3	49
134	Instance-Specific Accelerators for Minimum Covering. Journal of Supercomputing, 2003, 26, 109-129.	3.6	6
135	The case for reconfigurable hardware in wearable computing. Personal and Ubiquitous Computing, 2003, 7, 299-308.	2.8	27
136	Virtualizing Hardware with Multi-context Reconfigurable Arrays. Lecture Notes in Computer Science, 2003, , 151-160.	1.3	13
137	A Framework for Run-time Reconfigurable Systems. Journal of Supercomputing, 2002, 21, 145-159.	3.6	11
138	Object-oriented domain specific compilers for programming FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2001, 9, 205-210.	3.1	17
139	<title>Reconfigurable processors for handhelds and wearables: application analysis</title>. , 2001, , .		3
140	Reconfigurable accelerators for combinatorial problems. Computer, 2000, 33, 58-60.	1.1	16
141	Toward embedded qualitative simulation: a specialized computer architecture for QSim. IEEE Intelligent Systems, 2000, 15, 62-68.	0.2	5
142	Parallel qualitative simulation. Simulation Modelling Practice and Theory, 1997, 5, 623-638.	0.3	6