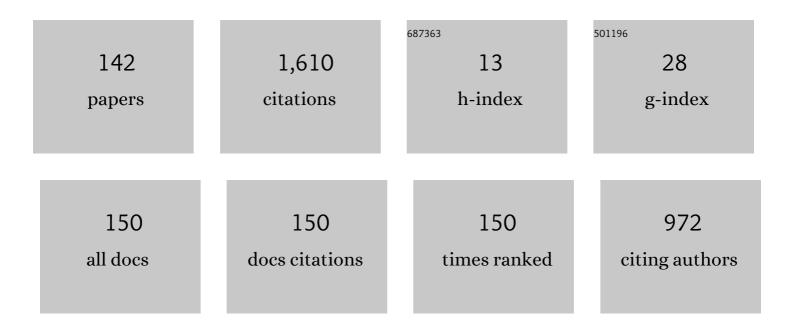
Marco Platzner

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/5694681/publications.pdf Version: 2024-02-01



#	Article	IF	CITATIONS
1	Operating systems for reconfigurable embedded platforms: online scheduling of real-time tasks. IEEE Transactions on Computers, 2004, 53, 1393-1407.	3.4	219
2	ReconOS. Transactions on Embedded Computing Systems, 2009, 9, 1-33.	2.9	121
3	ReconOS: An Operating System Approach for Reconfigurable Computing. IEEE Micro, 2014, 34, 60-71.	1.8	90
4	Fluctuating emg signals: Investigating long-term effects of pattern matching algorithms. , 2010, 2010, 6357-60.		82
5	Design and architectures for dependable embedded systems. , 2011, , .		73
6	ReconOS: An RTOS Supporting Hard-and Software Threads. , 2007, , .		50
7	A Runtime Environment for Reconfigurable Hardware Operating Systems. Lecture Notes in Computer Science, 2004, , 831-835.	1.3	49
8	Proof-Carrying Hardware: Towards Runtime Verification of Reconfigurable Modules. , 2009, , .		40
9	A self-adaptive heterogeneous multi-core architecture for embedded real-time video object tracking. Journal of Real-Time Image Processing, 2013, 8, 95-110.	3.5	34
10	The case for reconfigurable hardware in wearable computing. Personal and Ubiquitous Computing, 2003, 7, 299-308.	2.8	27
11	Executing Hardware Tasks on Dynamically Reconfigurable Devices Under Real-Time Conditions. , 2006, ,		24
12	An EDF schedulability test for periodic tasks on reconfigurable hardware devices. , 2006, , .		24
13	R-Codesign: Codesign Methodology for Real-Time Reconfigurable Embedded Systems Under Energy Constraints. IEEE Access, 2018, 6, 14078-14092.	4.2	23
14	EvoCaches: Application-specific Adaptation of Cache Mappings. , 2009, , .		22
15	Immersive augmented reality system for the training of pattern classification control with a myoelectric prosthesis. Journal of NeuroEngineering and Rehabilitation, 2021, 18, 25.	4.6	21
16	Towards robust HD EMG pattern recognition: Reducing electrode displacement effect using structural similarity. , 2014, 2014, 4547-50.		20
17	Cooperative multithreading in dynamically reconfigurable systems. , 2009, , .		19
18	Reducing classification accuracy degradation of pattern recognition based myoelectric control		19

caused by electrode shift using a high density electrode array. , 2012, 2012, 4324-7. 18

#	Article	IF	CITATIONS
19	Object-oriented domain specific compilers for programming FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2001, 9, 205-210.	3.1	17
20	Comparing Evolvable Hardware to Conventional Classifiers for Electromyographic Prosthetic Hand Control. , 2008, , .		17
21	Classification of Electromyographic Signals: Comparing Evolvable Hardware to Conventional Classifiers. IEEE Transactions on Evolutionary Computation, 2013, 17, 46-63.	10.0	17
22	Reconfigurable accelerators for combinatorial problems. Computer, 2000, 33, 58-60.	1.1	16
23	Seven recipes for setting your FPGA on fire – A cookbook on heat generators. Microprocessors and Microsystems, 2014, 38, 911-919.	2.8	16
24	Self-Awareness as a Model for Designing and Operating Heterogeneous Multicores. ACM Transactions on Reconfigurable Technology and Systems, 2014, 7, 1-18.	2.5	15
25	CIRCA: Towards a modular and extensible framework for approximate circuit generation. Microelectronics Reliability, 2019, 99, 277-290.	1.7	15
26	System-level performance evaluation of reconfigurable processors. Microprocessors and Microsystems, 2005, 29, 63-73.	2.8	14
27	MOVES: A Modular Framework for Hardware Evolution. , 2007, , .		14
28	A portable abstraction layer for hardware threads. , 2008, , .		14
29	On-The-Fly Computing: A novel paradigm for individualized IT services. , 2013, , .		14
30	A hardware/software infrastructure for performance monitoring on LEON3 multicore platforms. , 2014, , .		14
31	Memory Virtualization for Multithreaded Reconfigurable Hardware. , 2011, , .		13
32	Virtualizing Hardware with Multi-context Reconfigurable Arrays. Lecture Notes in Computer Science, 2003, , 151-160.	1.3	13
33	A Comparison of Evolvable Hardware Architectures for Classification Tasks. Lecture Notes in Computer Science, 2008, , 22-33.	1.3	13
34	Achieving hardware security for reconfigurable systems on chip by a proof-carrying code approach. , 2011, , .		12
35	Reducing the limb position effect in pattern recognition based myoelectric control using a high density electrode array. , 2013, , .		12
36	Embedding FPGA overlays into configurable Systems-on-Chip: ReconOS meets ZUMA. , 2014, , .		12

#	Article	IF	CITATIONS
37	A Framework for Run-time Reconfigurable Systems. Journal of Supercomputing, 2002, 21, 145-159.	3.6	11
38	Proof-Carrying Hardware: Concept and Prototype Tool Flow for Online Verification. International Journal of Reconfigurable Computing, 2010, 2010, 1-11.	0.2	10
39	A Triple Hybrid Interconnect for Many-Cores: Reconfigurable Mesh, NoC and Barrier. , 2010, , .		10
40	Evolution of Electronic Circuits. Natural Computing Series, 2011, , 125-179.	2.2	10
41	Memory security in reconfigurable computers: Combining formal verification with monitoring. , 2014, , .		10
42	An FPGA-Based Reconfigurable Mesh Many-Core. IEEE Transactions on Computers, 2014, 63, 2919-2932.	3.4	10
43	An EDF schedulability test for periodic tasks on reconfigurable hardware devices. ACM SIGPLAN Notices, 2006, 41, 93-102.	0.2	9
44	A Many-Core Implementation Based on the Reconfigurable Mesh Model. , 2007, , .		9
45	FPGA-based acceleration of high density myoelectric signal processing. , 2015, , .		9
46	An MCTS-based Framework for Synthesis of Approximate Circuits. , 2018, , .		9
47	ReconROS: Flexible Hardware Acceleration for ROS2 Applications. , 2020, , .		9
48	FPGA Redundancy Configurations: An Automated Design Space Exploration. , 2014, , .		8
49	Adaptive Playouts in Monte-Carlo Tree Search with Policy-Gradient Reinforcement Learning. Lecture Notes in Computer Science, 2015, , 1-11.	1.3	8
50	Distributed Monte Carlo Tree Search: A Novel Technique and its Application to Computer Go. IEEE Transactions on Games, 2015, 7, 361-374.	1.4	8
51	Jump Search. , 2019, , .		8
52	DeepWind: An Accurate Wind Turbine Condition Monitoring Framework via Deep Learning on Embedded Platforms. , 2020, , .		8
53	Performance-Centric Scheduling with Task Migration for a Heterogeneous Compute Node in the Data Center. , 2016, , .		8
54	ARMLang: A language and compiler for programming reconfigurable mesh many-cores. , 2009, , .		7

#	Article	IF	CITATIONS
55	Parallel qualitative simulation. Simulation Modelling Practice and Theory, 1997, 5, 623-638.	0.3	6
56	Instance-Specific Accelerators for Minimum Covering. Journal of Supercomputing, 2003, 26, 109-129.	3.6	6
57	Comparison of Bayesian move prediction systems for Computer Go. , 2012, , .		6
58	Common fate graph patterns in Monte Carlo Tree Search for computer go. , 2014, , .		6
59	Programming models for reconfigurable manycore systems. , 2016, , .		6
60	Zynq-based acceleration of robust high density myoelectric signal processing. Journal of Parallel and Distributed Computing, 2019, 123, 77-89.	4.1	6
61	A Multithreaded Framework for Sequential Monte Carlo Methods on CPU/FPGA Platforms. Lecture Notes in Computer Science, 2009, , 380-385.	1.3	6
62	ReconOS: An Operating System forÂDynamically Reconfigurable Hardware. , 2010, , 269-290.		6
63	Toward embedded qualitative simulation: a specialized computer architecture for QSim. IEEE Intelligent Systems, 2000, 15, 62-68.	0.2	5
64	Server-based execution of periodic tasks on dynamically reconfigurable hardware. IET Computers and Digital Techniques, 2007, 1, 295.	1.2	5
65	An adaptive Sequential Monte Carlo framework with runtime HW/SW repartitioning. , 2009, , .		5
66	An accelerator for K-TH nearest neighbor thinning based on the IMORC infrastructure. , 2009, , .		5
67	A novel hybrid evolutionary strategy and its periodization with multi-objective genetic optimizers. , 2010, , .		5
68	Adaptive playouts for online learning of policies during Monte Carlo Tree Search. Theoretical Computer Science, 2016, 644, 53-62.	0.9	5
69	Self-aware Computing: Introduction and Motivation. Natural Computing Series, 2016, , 1-5.	2.2	5
70	Coping with Resource Fluctuations: The Run-time Reconfigurable Functional Unit Row Classifier Architecture. Lecture Notes in Computer Science, 2010, , 250-261.	1.3	5
71	Realizing reconfigurable mesh algorithms on softcore arrays. , 2008, , .		4
72	IMORC: Application Mapping, Monitoring and Optimization for High-Performance Reconfigurable Computing. , 2009, , .		4

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#	Article	IF	CITATIONS
73	Improving transient state myoelectric signal recognition in hand movement classification using gyroscopes. , 2013, 2013, 6035-8.		4
74	Proof-Carrying Hardware via Inductive Invariants. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-23.	2.6	4
75	Computational self-awareness as design approach for visual sensor nodes. , 2017, , .		4
76	An Approach for Mapping Periodic Real-Time Tasks to Reconfigurable Hardware. , 2019, , .		4
77	Proof-Carrying Hardware Versus the Stealthy Malicious LUT Hardware Trojan. Lecture Notes in Computer Science, 2019, , 127-136.	1.3	4
78	Dynamic Reliability Management for FPGA-Based Systems. International Journal of Reconfigurable Computing, 2020, 2020, 1-19.	0.2	4
79	On Robust Evolution of Digital Hardware. International Federation for Information Processing, 2008, , 213-222.	0.4	4
80	Design of Distributed Reconfigurable Robotics Systems with ReconROS. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-20.	2.5	4
81	MUSCAT: MUS-based Circuit Approximation Technique. , 2022, , .		4
82	<title>Reconfigurable processors for handhelds and wearables: application analysis</title> ., 2001, , .		3
83	IMORC: An infrastructure and architecture template for implementing high-performance reconfigurable FPGA accelerators. Microprocessors and Microsystems, 2012, 36, 110-126.	2.8	3
84	Dynamic reliability management: Reconfiguring reliability-levels of hardware designs at runtime. , 2013, , .		3
85	Evaluating fault-tolerance of redundant FPGA structures using Boolean difference calculus. Microprocessors and Microsystems, 2017, 52, 160-172.	2.8	3
86	reMinMin: A novel static energy-centric list scheduling approach based on real measurements. , 2017, , .		3
87	Combining Local and Global Search: A Multi-objective Evolutionary Algorithm for Cartesian Genetic Programming. Emergence, Complexity and Computation, 2018, , 175-194.	0.3	3
88	Using Deep Convolutional Neural Networks in Monte Carlo Tree Search. Lecture Notes in Computer Science, 2016, , 11-21.	1.3	3
89	New Co-design Methodology for Real-time Embedded Systems. , 2016, , .		3
90	Performance estimation framework for automated exploration of CPU-accelerator architectures. , 2011, , .		2

#	Article	IF	CITATIONS
91	Towards self-adaptive caches: A run-time reconfigurable multi-core infrastructure. , 2014, , .		2
92	Analytic reliability evaluation for fault-tolerant circuit structures on FPGAs. , 2014, , .		2
93	Microarchitectural optimization by means of reconfigurable and evolvable cache mappings. , 2015, , .		2
94	An architecture and design tool flow for embedding a virtual FPGA into a reconfigurable system-on-chip. Computers and Electrical Engineering, 2016, 55, 112-122.	4.8	2
95	On-the-fly computing. , 2016, , .		2
96	A Zynq-based dynamically reconfigurable high density myoelectric prosthesis controller. , 2017, , .		2
97	Ampehre: An Open Source Measurement Framework for Heterogeneous Compute Nodes. Lecture Notes in Computer Science, 2018, , 73-84.	1.3	2
98	Hardware Virtualization on Dynamically Reconfigurable Processors. , 2011, , 82-109.		2
99	Multi-objective Intrinsic Evolution of Embedded Systems. , 2011, , 193-206.		2
100	On Semeai Detection in Monte-Carlo Go. Lecture Notes in Computer Science, 2014, , 14-25.	1.3	2
101	Integrating Software and Hardware Verification. Lecture Notes in Computer Science, 2014, , 307-322.	1.3	2
102	Thread Shadowing: Using Dynamic Redundancy on Hybrid Multi-cores for Error Detection. Lecture Notes in Computer Science, 2014, , 283-290.	1.3	2
103	Software/Hardware Co-Verification for Custom Instruction Set Processors. IEEE Access, 2021, 9, 160559-160579.	4.2	2
104	Optimal temporal partitioning based on slowdown and retiming. , 2006, , .		1
105	SPP1148 booth: Fine grain reconfigurable architectures. , 2008, , .		1
106	Communication Performance Characterization for Reconfigurable Accelerator Design on the XD1000. , 2009, , .		1
107	Engineering self-coordinating software intensive systems. , 2010, , .		1
108	Reconfigurable nodes for future networks. , 2010, , .		1

108 Reconfigurable nodes for future networks. , 2010, , .

109 PRGA Acceleration of Communication-Bound Streaming Applications: Architecture Modeling and a 30 0.2 1 110 Significant papers from the first 25 years of the FPL conference., 2015, 1 111 Comparison of thread signatures for error detection in hybrid multi-cores, 2015, 1 112 Monte-Carlo simulation balancing revisited., 2016, 1 113 Thread shadowing: On the effectiveness of error detection at the hardware thread level, 2016, 1 114 Hardware, 2016, 1 115 Self-aware Compute Nodes. Natural Computing Series, 2016, 1 116 Accurate private/based classification of memory accesses: A run-time analysis system for the LEON3 2.2 1 116 Accurate private/based classification on memory accesses: A run-time analysis system for the LEON3 2.5 1 117 Systems, 2017, 10, 1-17. 1 1 118 Computing Diot Specification of memory accesses: A run-time analysis system for the LEON3 2.5 1 119 Systems, 2017, 10, 1-17. 1 1 1 119 Courst Effortabil EEE Transactions on Computers and EEE Transactions on Emerging Topics in Som Marker for proves on Computers and EEE Transacting compute Nodes, 2020,	#	Article	IF	CITATIONS
111 Comparison of thread signatures for error detection in hybrid multi-cores., 2015, 1 112 Monte Carlo simulation balancing revisited., 2016, 1 113 Thread shadowing: On the effectiveness of error detection at the hardware thread level., 2016, 1 114 Verifying worst-case completion times for reconfigurable hardware modules using proof-carrying 1 115 Self-aware Compute Nodes. Natural Computing Series, 2016, , 145-165. 2.2 1 116 Accurate private/datared classification of memory accesses: A run-time analysis system for the LEON3 1 117 Type protection at the PPL Conference. ACM Transactions on Reconfigurable Technology and 2.5 1 118 Computing Joint Special Section on Inmovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Emerging Topics in Computing Joint Special Section on Inmovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Emerging Topics in Computing. 2017, 5, 207-209. 1 119 Altight Accurate Energy Model for Task Execution on Heterogeneous Compute Nodes., 2020, 1 120 MigHEFT: DAG-based Scheduling of Migratable Tasks on Heterogeneous Compute Nodes., 2020, 1 121 Exploiting Hardware-Based Data Parallel and Multithreading Models for Smart Edge Computing In Reconfigurable PrOAs. IEEE Transactions on Computers. 2022, 7, 1, 2003-	109	FPGA Acceleration of Communication-Bound Streaming Applications: Architecture Modeling and a 3D Image Compositing Case Study. International Journal of Reconfigurable Computing, 2011, 2011, 1-11.	0.2	1
112 Monte-Carlo simulation balancing revisited., 2016, , . 1 113 Thread shadowing: On the effectiveness of error detection at the hardware thread level., 2016, , . 1 114 Verifying worst-case completion times for reconfigurable hardware modules using proof-carrying 1 115 Self-aware Compute Nodes. Natural Computing Series, 2016, , 145-165. 2.2 1 116 Accurate private/shared classification of memory accesses: A run-time analysis system for the LEON3 1 117 The First 25 Years of the FPL Conference. ACM Transactions on Reconfigurable Technology and Systems, 2017, 10, 1-17. 1 118 Computing biot Specifies Section on Immovation in Reconfigurable Technology and Systems, 2017, 10, 1-17. 4.6 1 119 Artightly Accurate Energy Model for Task Execution on Heterogeneous Compute Nodes., 2018, 1 120 MigHEFF: DAG-based Scheduling of Migratable Tasks on Heterogeneous Compute Nodes., 2018, 1 121 Exploiting Hardware-Based Data-Paraliel and Multithreading Models for Smart Edge Computing in Section on Immovition in Reconfigurable Computing in Section Seconfigurable PGAs. Section Seconfigurable Models for Sma	110	Significant papers from the first 25 years of the FPL conference. , 2015, , .		1
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120 MigHEFT: DAG-based Scheduling of Migratable Tasks on Heterogeneous Compute Nodes., 2020, , . 1 121 Exploiting Hardware-Based Data-Parallel and Multithreading Models for Smart Edge Computing in Reconfigurable FPGAs. IEEE Transactions on Computers, 2022, 71, 2903-2914. 3.4 1 122 <i>LDAX 1 1 123 MCTS-based Synthesis Towards Efficient Approximate Accelerators., 2021, , . 1 124 On-The-Fly Verification of Reconfigurable Image Processing Modules Based on a Proof-Carrying Hardware Approach. Lecture Notes in Computer Science, 2015, , 365-372. 1.3 1</i>	118	Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to	4.6	1
121 Exploiting Hardware-Based Data-Parallel and Multithreading Models for Smart Edge Computing in Reconfigurable FPGAs. IEEE Transactions on Computers, 2022, 71, 2903-2914. 3.4 1 122 <i>LDAX</i> , 2021, ,. 1 123 MCTS-based Synthesis Towards Efficient Approximate Accelerators., 2021, ,. 1 124 On-The-Fly Verification of Reconfigurable Image Processing Modules Based on a Proof-Carrying Hardware Approach. Lecture Notes in Computer Science, 2015, , 365-372. 1.3 1	119	A Highly Accurate Energy Model for Task Execution on Heterogeneous Compute Nodes. , 2018, , .		1
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#	Article	IF	CITATIONS
127	Optimization of Application-Specific L1 Cache Translation Functions of the LEON3 Processor. Advances in Intelligent Systems and Computing, 2021, , 266-276.	0.6	1
128	A Hybrid Synthesis Methodology for Approximate Circuits. , 2020, , .		1
129	Dynamically Reconfigurable Architectures. Eurasip Journal on Embedded Systems, 2007, 2007, 1-2.	1.2	0
130	Program-driven fine-grained power management for the reconfigurable mesh. , 2009, , .		0
131	Boolean Difference Based Reliability Evaluation of Fault-Tolerant Circuit Structures on FPGAs. , 2016, , \cdot		Ο
132	Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing Joint Special Section on Innovation in Reconfigurable Computing Fabrics from Devices to Architectures. IEEE Transactions on Computers, 2017, 66, 927-929.	3.4	0
133	Evaluation methodology for complex non-deterministic functions: A case study in metaheuristic optimization of caches. , 2017, , .		0
134	Evolvable caches: Optimization of reconfigurable cache mappings for a LEON3/Linux-based multi-core processor. , 2017, , .		0
135	An Accelerator for Resolution Proof Checking based on FPGA and Hybrid Memory Cube Technology. Journal of Signal Processing Systems, 2019, 91, 1259-1272.	2.1	Ο
136	Evolution of application-specific cache mappings. International Journal of Hybrid Intelligent Systems, 2020, 16, 149-161.	1.2	0
137	Proof-Carrying Approximate Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2084-2088.	3.1	Ο
138	Timing Optimization for Virtual FPGA Configurations. Lecture Notes in Computer Science, 2021, , 50-64.	1.3	0
139	Multithreaded Programming of Reconfigurable Embedded Systems. , 2011, , 31-54.		Ο
140	Compensating Resource Fluctuations by Means of Evolvable Hardware. International Journal of Adaptive Resilient and Autonomic Systems, 2012, 3, 17-31.	0.3	0
141	I-Codesign: A Codesign Methodology for Reconfigurable Embedded Systems. Communications in Computer and Information Science, 2017, , 153-174.	0.5	0
142	An FPGA/HMC-Based Accelerator forÂResolution Proof Checking. Lecture Notes in Computer Science, 2018, , 153-165.	1.3	0