Xiaowu Zhang

List of Publications by Year
in descending order

97 papers	1,906 citations	331670 21 h-index	289244 40 g-index
97 all docs	97 docs citations	97 times ranked	1326 citing authors

#	Article	IF	Citations
1	Nonlinear Thermal Stress/Strain Analyses of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps. IEEE Transactions on Advanced Packaging, 2009, 32, 720-728.	1.6	229
2	High-Density 3D-Boron Nitride and 3D-Graphene for High-Performance Nanoâ€“Thermal Interface Material. ACS Nano, 2017, 11, 2033-2044.	14.6	152
3	The study of mechanical properties of Snâ€“Agâ€“Cu lead-free solders with different Ag contents and Ni doping under different strain rates and temperatures. Journal of Alloys and Compounds, 2010, 507, 215-224.	5.5	135
4	Heterogeneous 2.5D integration on through silicon interposer. Applied Physics Reviews, 2015, 2, 021308.	11.3	108
5	Development of 3-D Silicon Module With TSV for System in Packaging. IEEE Transactions on Components and Packaging Technologies, 2010, 33, 3-9.	1.3	91
6	Study on Cu Protrusion of Through-Silicon Via. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 732-739.	2.5	74
7	Electromigration performance of Through Silicon Via (TSV) â€“ A modeling approach. Microelectronics Reliability, 2010, 50, 1336-1340.	1.7	63
8	Development of Wafer-Level Warpage and Stress Modeling Methodology and Its Application in Process Optimization for TSV Wafers. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012, 2, 944-955.	2.5	50
9	Thermal Management of Hotspots With a Microjet-Based Hybrid Heat Sink for GaN-on-Si Devices. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1441-1450.	2.5	38
10	Enhancement of Hotspot Cooling With Diamond Heat Spreader on Cu Microchannel Heat Sink for GaN-on-Si Device. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 983-990.	2.5	37
11	Development of Large Die Fine-Pitch Cu/Low-k FCBGA Package With Through Silicon via (TSV) Interposer. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 660-672.	2.5	35
12	Reliability study of 3D IC packaging based on through-silicon interposer (TSI) and silicon-less interconnection technology (SLIT) using finite element analysis. Microelectronics Reliability, 2016, 61, 64-70.	1.7	35
13	Thermo-mechanical finite element analysis in a multichip build up substrate based package design. Microelectronics Reliability, 2004, 44, 611-619.	1.7	34
14	Modeling Stress in Silicon With TSVs and Its Effect on Mobility. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 1328-1335.	2.5	33
15	A Damage Evolution Model for Thermal Fatigue Analysis of Solder Joints. Journal of Electronic Packaging, Transactions of the ASME, 2000, 122, 200-206.	1.8	32
16	Application of piezoresistive stress sensors in ultra thin device handling and characterization. Sensors and Actuators A: Physical, 2009, 156, 2-7.	4.1	31
17	Thermal Management of Hotspots Using Diamond Heat Spreader on Si Microcooler for GaN Devices. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1740-1746.	2.5	29
18	Si-Based Hybrid Microcooler With Multiple Drainage Microtrenches for High Heat Flux Cooling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 50-57.	2.5	27

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19	Numerical Study of Gold Wire Bonding Process on Cu/Low-k Structures. IEEE Transactions on Advanced Packaging, 2007, 30, 448-456.	1.6	26
20	Design and fabrication of a reliability test chip for 3D-TSV. , 2010, , .		23
21	Residual Stress Analysis in Thin Device Wafer Using Piezoresistive Stress Sensor. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 841-851.	2.5	22
22	Thermal Optimization and Characterization of SiC-Based High Power Electronics Packages With Advanced Thermal Design. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 854-863.	2.5	22
23	Investigation on Die Shift Issues in the 12-in Wafer-Level Compression Molding Process. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 1647-1653.	2.5	21
24	Creep Properties of Sn-1.0Ag-0.5Cu Lead-Free Solder with Ni Addition. Journal of Electronic Materials, 2011, 40, 344-354.	2.2	20
25	In Situ Measurement and Stress Evaluation for Wire Bonding Using Embedded Piezoresistive Stress Sensors. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 328-335.	2.5	20
26	3-D Numerical and Experimental Investigations on Compression Molding in Multichip Embedded Wafer Level Packaging. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 678-687.	2.5	18
27	Comprehensive Study on the Interactions of Multiple Die Shift Mechanisms During Wafer Level Molding of Multichip-Embedded Wafer Level Packages. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1090-1098.	2.5	18
28	Package-Level Microjet-Based Hotspot Cooling Solution for Microelectronic Devices. IEEE Electron Device Letters, 2015, 36, 502-504.	3.9	18
29	Green and efficient production of boron nitride nanosheets via oxygen doping-facilitated liquid exfoliation. Ceramics International, 2019, 45, 4909-4917.	4.8	18
30	Trapezoidal Microchannel Heat Sink With Pressure-Driven and Electro-Osmotic Flows for Microelectronic Cooling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 1851-1858.	2.5	17
31	Thermo-Mechanical Design Rules for the Fabrication of TSV Interposers. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 633-640.	2.5	17
32	Package-level Si-based micro-jet impingement cooling solution with multiple drainage micro-trenches. , 2014, , .		17
33	Stress Analysis and Design Optimization for Low-<inline-formula> <tex-math notation="LaTeX">k </tex-math></inline-formula> Chip With Cu Pillar Interconnection. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1273-1283.	2.5	17
34	Sensitivity study on material properties for the fatigue life prediction of solder joints under cyclic thermal loading. Circuit World, 1998, 24, 26-31.	0.9	16
35	Board level solder joint reliability analysis of a fine pitch Cu post type wafer level package (WLP). Microelectronics Reliability, 2008, 48, 602-610.	1.7	16
36	Structure Design Optimization and Reliability Analysis on a Pyramidal-Shape Three-Die-Stacked Package With Through-Silicon Via. IEEE Transactions on Device and Materials Reliability, 2012, 12, 201-208.	2.0	15

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37	Clarification of Stress Field Measured by Multiwavelength Micro-Raman Spectroscopy in the Surrounding Silicon of Copper-Filled Through-Silicon Vias. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1010-1014.	2.5	14
38	Computational parametric analyzes on the solder joint reliability of bottom leaded plastic (BLP) package. IEEE Transactions on Advanced Packaging, 2002, 25, 514-521.	1.6	13
39	Development of process modeling methodology for flip chip on flex interconnections with non-conductive adhesives. Microelectronics Reliability, 2005, 45, 1215-1221.	1.7	13
40	Development of a Compact and Efficient Liquid Cooling System With Silicon Microcooler for High-Power Microelectronic Devices. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 729-739.	2.5	13
41	Hybrid micro-fluid heat sink for high power dissipation of liquid-cooled data centre. , 2017, , .		13
42	Si Microfluid Cooler With Jet-Slot Array for Server Processor Direct Liquid Cooling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 255-262.	2.5	13
43	Characterization and Modeling of Fine-Pitch Copper Ball Bonding on a Cu/Low-k Chip. Journal of Electronic Materials, 2015, 44, 688-698.	2.2	12
44	Design and Development of Fine Pitch Copper/Low-K Wafer Level Package. IEEE Transactions on Advanced Packaging, 2010, 33, 377-388.	1.6	11
45	A Thermal Isolation Technique Using Through-Silicon Vias for Three-Dimensional ICs. IEEE Transactions on Electron Devices, 2013, 60, 1282-1287.	3.0	11
46	Development of a jet-based Si micro-cooler with multiple drainage micro-trenches. , 2015, , .		10
47	Development of a Novel Lead Frame Based Double Side Liquid Cooling High Performance SiC Power Module. , 2021, , .		10
48	Application of Piezoresistive Stress Sensor in Wafer Bumping and Drop Impact Test of Embedded Ultrathin Device. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012, 2, 935-943.	2.5	9
49	Dynamic Mechanical Analysis and Viscoelastic Behavior of Epoxy Molding Compounds Used in Fan-Out Wafer-Level Packaging. , 2018, , .		9
50	Evaluation of Stresses in Thin Device Wafer using Piezoresistive Stress Sensor. , 2008, , .		8
51	Enhancement of Silicon-Based Inductor Q-Factor Using Polymer Cavity. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012, 2, 1973-1979.	2.5	8
52	Thermal management of hotspots using upstream laminar micro-jet impinging array. , 2013, , .		8
53	Effect of Boron Nitride Nanosheets on Properties of a Commercial Epoxy Molding Compound Used in Fan-Out Wafer-Level Packaging. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 990-999.	2.5	8
54	Reliability Evaluation for Copper/Low-k Structures Based on Experimental and Numerical Methods. IEEE Transactions on Device and Materials Reliability, 2008, 8, 455-463.	2.0	7

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55	Low-Stress Bond Pad Design for Low-Temperature Solder Interconnections on Through-Silicon Vias (TSVs). IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 510-518.	2.5	7
56	Underfill Selection, Characterization, and Reliability Study for Fine-Pitch, Large Die Cu/Low-K Flip Chip Package. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 279-290.	2.5	7
57	Study on the Effect of Wafer Back Grinding Process on Nanomechanical Behavior of Multilayered Low-k Stack. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012, 2, 3-12.	2.5	7
58	Design, assembly and reliability of large die and fine-pitch Cu/low-k flip chip package. Microelectronics Reliability, 2010, 50, 986-994.	1.7	6
59	Development of a Cu/Low-k Stack Die Fine Pitch Ball Grid Array (FBGA) Package for System in Package Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 299-309.	2.5	6
60	Design and Optimization of Wafer-Level Compression Molding Process for One Chip Plus Multiple Decaps. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 606-613.	2.5	6
61	Board level solder joint life prediction of fine pitch large IC. , 2006, , .		5
62	Mapping the failure envelope of board-level solder joints. Microelectronics Reliability, 2009, 49, 397-409.	1.7	5
63	Modular sensor chip design for package stress evaluation and reliability characterisation. Microelectronics Reliability, 2012, 52, 1581-1585.	1.7	5
64	Heat Dissipation Capability of a Package-on-Package Embedded Wafer-Level Package. IEEE Design and Test, 2015, 32, 32-39.	1.2	5
65	Package Level Warpage Simulation of Fan-out Wafer Level Package (FOWLP) Considering Viscoelastic Material Properties. , 2018, , .		5
66	Design, Fabrication and Characterization of a Mini Heat Exchanger for Data Centre Cooling Application. , 2018, , .		5
67	Selective interactions of glycidylamine epoxy/boron nitride nanosheets as a facile method to reinforce bisphenol-A epoxy resins. Polymer, 2020, 202, 122626.	3.8	5
68	Impact of Packaging Design on Reliability of Large Die Cu/Low-$kappa$ (BD) Interconnect. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012, 2, 807-816.	2.5	4
69	Investigation on Reliability of Embedded Ultrathin Sensor Chip in Organic Substrate Under Drop Impact Loading by Stresses Monitor and FEM Simulation. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1309-1316.	2.5	4
70	An efficient single phase liquid cooling system for microelectronic devices with high power chip. , 2015, , .		4
71	Design of Micro-sensors for Measuring Localised Stresses during Fan-Out Wafer Level Packaging (FOWLP) Processes. , 2018, , .		4
72	Effect of Thermal Cycling on the Thermal and Mechanical Properties of Dielectric Materials. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1166-1174.	2.5	4

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73	A Dynamic Control System for Server Processor Direct Liquid Cooling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 786-794.	2.5	4
74	Board Level Reliability Enhancement for A Double-bump Wafer Level Chip Scale Package. Journal of Microelectronics and Electronic Packaging, 2004, 1, 64-71.	0.7	4
75	Structural Design and Optimization of 65nm Cu/low-k Flipchip Package. , 2007, , .		3
76	Integrated Process-Aging Modeling Methodology for Flip Chip on Flex Interconnections With Nonconductive Adhesives. IEEE Transactions on Advanced Packaging, 2008, 31, 882-889.	1.6	3
77	Modeling and characterization of Cu wire bonding process on silicon chip with 45nm node and Cu/low-k structures. , 2013, , .		3
78	Micro-channel heat sink with multiple interactive pressure-driven or electro-osmotic flows. , 2015, , .		3
79	Heat dissipation improvement with diamond heat spreader on hybrid Si micro-cooler for GaN devices. , 2015, , .		3
80	Si-Based Hybrid Microfluidic Cooling for Server Processor of Data Centre. , 2018, , .		3
81	Investigation of Liquid Cooling for Data Center Server Based on Micro-fluid Technology. , 2019, , .		3
82	Development of Advanced Liquid Cooling Solution on Data Centre Cooling. , 2022, , .		3
83	Modeling and Control of Hybrid Si-Based Micro-Fluid Cooling System for Data Center Application. , 2018, , .		2
84	Application of Piezoresistive Stress Sensor in Mold-1st Fan-out Wafer Level Packaging Processes. , 2019, , .		2
85	Modeling and Deep Explicit Model Predictive Control for Server Processor Direct Liquid Cooling. , 2019, , .		2
86	Addressing Warpage Issue and Reliability Challenge of Fan-out Wafer-Level Packaging (FOWLP). , 2021, , .		2
87	Thermo-mechanical design of large die fine pitch copper/low-k FCBGA and lead-free interconnections. , 2008, , .		1
88	Investigation on decap shift and incomplete fill issues in the wafer level compression molding process. , 2013, , .		1
89	Design Optimization and Characterization of Silicon Microcooler System Through Finite-Element Modeling and Experimental Analyses. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 224-237.	2.5	1
90	Thermal design and analysis of through silicon interposer (TSI) package. , 2017, , .		1

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91	Mold Flow Simulation for Fan-out Panel-Level Packaging (FOPLP). , 2018, , .		1
92	Comprehensive Design and Analysis of Fan-Out Wafer Level Package. , 2019, , .		1
93	Thermal Analysis and Material Selection of the SiC Based Intelligent Power Package. , 2019, , .		1
94	Nonlinear Thermal Stress/Strain Analyses of Through SiC Via. , 2021, , .		1
95	Design and development of micro-sensors for measuring localised stresses during copper wirebonding. , 2012, , .		0
96	Study on dynamic modeling and reliability analysis of wafer thinning process for TSV wafer. , 2013, , .		0
97	Development of Thermal Test Package for Data Center Micro-Fluid Cooling Characterization. , 2018, , .		0