Chen-Yi Lee

List of Publications by Year
in descending order

221 papers	3,487 citations	201674 27 h-index	197818 49 g-index
221 all docs	221 docs citations	221 times ranked	1935 citing authors

#	Article	IF	Citations
1	A Traveling-Wave Dielectrophoresis Bio-Chip for Cell Manipulation in Standard CMOS Process. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1582-1586.	3.0	4
2	A Programmable Bio-Chip With Adaptive Pattern-Control Micro-Electrode-Dot-Array. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4513-4517.	3.0	3
3	Betel quid chewing and cessation in the sociocultural context of Paiwan people from Taiwan: a qualitative study. Journal of Ethnicity in Substance Abuse, 2021, 20, 395-414.	0.9	3
4	Optimizing Residual Networks and VGG for Classification of EEG Signals: Identifying Ideal Channels for Emotion Recognition. Journal of Healthcare Engineering, 2021, 2021, 1-14.	1.9	22
5	PPG-Based Smart Wearable Device With Energy-Efficient Computing for Mobile Health-Care Applications. IEEE Sensors Journal, 2021, 21, 13564-13573.	4.7	24
6	The impact of the COVID-19 epidemic on the utilization of dental services and attitudes of dental residents at the emergency department of a medical center in Taiwan. Journal of Dental Sciences, 2021, 16, 868-876.	2.5	14
7	Development and questionnaire-based evaluation of virtual dental clinic: a serious game for training dental students. Medical Education Online, 2021, 26, 1983927.	2.6	8
8	Convolutional neural networks for classification of music-listening EEG: comparing 1D convolutional kernels with 2D kernels and cerebral laterality of musical influence. Neural Computing and Applications, 2020, 32, 8867-8891.	5.6	24
9	Multitarget Sample Preparation Using MEDA Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2682-2695.	2.7	11
10	NeuralScale: Efficient Scaling of Neurons for Resource-Constrained Deep Neural Networks. , 2020, , .		7
11	Utilization of silicon nanowire field-effect transistors for the detection of a cardiac biomarker, cardiac troponin I and their applications involving animal models. Scientific Reports, 2020, 10, 22027.	3.3	19
12	Cross-Domain Adaptation for Biometric Identification Using Photoplethysmogram. , 2020, , .		8
13	Deep learning assisted detection of glaucomatous optic neuropathy and potential designs for a generalizable model. PLoS ONE, 2020, 15, e0233079.	2.5	22
14	Reduction of Contact Resistivity by Nano-Textured Contact. Journal of Electronic Materials, 2020, 49, 6783-6788.	2.2	0
15	Feature Consistency Training With JPEG Compressed Images. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 4769-4780.	8.3	11
16	Effects of anxiety on dental students' noncognitive performance in their first objective structured clinical examination. Kaohsiung Journal of Medical Sciences, 2020, 36, 850-856.	1.9	9
17	FADE: Feature Aggregation for Depth Estimation With Multi-View Stereo. IEEE Transactions on Image Processing, 2020, 29, 6590-6600.	9.8	5
18	Energy Harvesting For Wearable Devices: A Review. IEEE Sensors Journal, 2019, 19, 9047-9062.	4.7	130

#	Article	IF	Citations
19	Joint Capacitive Sensing and Frequency Selection for Fast Medical Tests. , 2019, , .		0
20	A Lightweight 1.16 pJ/bit Processor for the Authenticated Encryption Scheme KetjeSR. , 2019, , .		0
21	Centralized State Sensing using Sensor Array on Wearable Device. , 2019, , .		3
22	Work stress and occupational burnout among dental staff in a medical center. Journal of Dental Sciences, 2019, 14, 295-301.	2.5	30
23	Sample preparation for multiple-reactant bioassays on micro-electrode-dot-array biochips. , 2019, , .		11
24	Micro-Electrode-Dot-Array Digital Microfluidic Biochips: Technology, Design Automation, and Test Techniques. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 292-313.	4.0	38
25	Structural and Functional Test Methods for Micro-Electrode-Dot-Array Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 968-981.	2.7	21
26	Efficient and Adaptive Error Recovery in a Micro-Electrode-Dot-Array Digital Microfluidic Biochip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 601-614.	2.7	30
27	Ultrasensitive Electrical Detection of Follicle-Stimulating Hormone Using a Functionalized Silicon Nanowire Transistor Chemosensor. ACS Applied Materials & Interfaces, 2018, 10, 36120-36127.	8.0	11
28	Diabetic Retinopathy Detection Based on Deep Convolutional Neural Networks. , 2018, , .		37
29	Confnet: Predict with Confidence. , 2018, , .		8
30	UAVNet: An Efficient Obstacel Detection Model for UAV with Autonomous Flight. , 2018, , .		7
31	A Fully Integrated 16-Channel Closed-Loop Neural-Prosthetic CMOS SoC With Wireless Power and Bidirectional Data Telemetry for Real-Time Efficient Human Epileptic Seizure Control. IEEE Journal of Solid-State Circuits, 2018, 53, 3314-3326.	5.4	92
32	Qualitative study for betel quid cessation among oral cancer patients. PLoS ONE, 2018, 13, e0199503.	2.5	10
33	Droplet Size-Aware High-Level Synthesis for Micro-Electrode-Dot-Array Digital Microfluidic Biochips. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 612-626.	4.0	50
34	Sample Preparation on Micro-Electrode-Dot-Array Digital Microfluidic Biochips. , 2017, , .		13
35	An Improved DPA Countermeasure Based on Uniform Distribution Random Power Generator for IoT Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2522-2531.	5.4	7
36	Droplet Size-Aware and Error-Correcting Sample Preparation Using Micro-Electrode-Dot-Array Digital Microfluidic Biochips. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1380-1391.	4.0	20

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37	Betel Quid Dependence Scale. , 2016, , 827-835.		1
38	A 41.3pJ/26.7pJ per neuron weight RBM processor for on-chip learning/inference applications. , 2016, , .		1
39	A 7.72 Gb/s LDPC-CC decoder with overlapped architecture for pre-5G wireless communications. , 2016, , .		4
40	Design of a micro-electrode cell for programmable lab-on-CMOS platform. , 2016, , .		28
41	Built-in self-test for micro-electrode-dot-array digital microfluidic biochips. , 2016, , .		21
42	A multi-axis readout circuit using in female ovulation monitoring platform. , 2016, , .		1
43	An Efficient Decoder Architecture for Nonbinary LDPC Codes With Extended Min-Sum Algorithm. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 863-867.	3.0	17
44	Patterns of Betel Quid, Cigarette, and Alcohol Use, and Their Correlates With Betel Quid Cessation in a Male Inmate Population. Substance Use and Misuse, 2016, 51, 471-478.	1.4	10
45	A field-programmable lab-on-a-chip with built-in self-test circuit and low-power sensor-fusion solution in 0.35Î¼m standard CMOS process. , 2015, , .		24
46	A 1.31Gb/s, 96.6% utilization stochastic nonbinary LDPC decoder for small cell applications. , 2015, , .		0
47	Reasons for Permanent Tooth Extractions in Taiwan. Asia-Pacific Journal of Public Health, 2015, 27, NP2350-NP2357.	1.0	22
48	A 3.46 Gb/s (9141,8224) LDPC-based ECC scheme and on-line channel estimation for solid-state drive applications. , 2015, , .		7
49	An Intelligent Digital Microfluidic Processor for Biomedical Detection. Journal of Signal Processing Systems, 2015, 78, 85-93.	2.1	71
50	An MPCN-Based BCH Codec Architecture With Arbitrary Error Correcting Capability. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1235-1244.	3.1	4
51	An OFDM-based 29.1Mbps 0.22nJ/bit body channel communication baseband transceiver. , 2015, , .		7
52	Jointly Designed Nonbinary LDPC Convolutional Codes and Memory-Based Decoder Architecture. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2523-2532.	5.4	1
53	A Hardware-Efficient Sigmoid Function With Adjustable Precision for a Neural Network System. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 1073-1077.	3.0	52
54	An Area-Efficient Relaxed Half-Stochastic Decoding Architecture for Nonbinary LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 301-305.	3.0	3

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55	Efficient Hardware Architecture of <inline-formula> <tex-math notation="LaTeX">eta_{T} </tex-math></inline-formula> Pairing Accelerator Over Characteristic Three. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 88-97.	3.1	2
56	A 1–100Mb/s 0.5–9.9mW LDPC convolutional code decoder for body area network. , 2014, , .		3
57	Event-driven read-out circuits for energy-efficient sensor-SoC's. , 2014, , .		0
58	A 2 GOPS quad-mean shift processor with early termination for machine learning applications. , 2014, , .		2
59	A 3.3V 15.6b 6.1pJ/0.02%RH with 10ms response humidity sensor for respiratory monitoring. , 2014, , .		2
60	Fieldâ€programmable labâ€onâ€aâ€chip based on microelectrode dot array architecture. IET Nanobiotechnology, 2014, 8, 163-171.	3.8	55
61	Area-efficient TFM-based stochastic decoder design for non-binary LDPC codes. , 2014, , .		7
62	A digital microfluidic processor for biomedical applications. , 2013, , .		6
63	A 3.66Gb/s 275mW TB-LDPC-CC decoder chip for MIMO broadcasting communications. , 2013, , .		6
64	A 446.6K-gates 0.55–1.2V H.265/HEVC decoder for next generation video applications. , 2013, , .		7
65	Strengthening Modern Electronics Industry Through the National Program for Intelligent Electronics in Taiwan. IEEE Access, 2013, 1, 123-130.	4.2	3
66	Extrinsic data compression method for double-binary turbo codes. , 2012, , .		1
67	A memory-efficient architecture for intra predictor and de-blocking filter in video coding system. , 2012, , .		0
68	A sub-100µW multi-functional cardiac signal processor for mobile healthcare applications. , 2012, , .		12
69	A (50,2,4) nonbinary LDPC convolutional code decoder chip over GF(256) in 90nm CMOS. , 2012, , .		1
70	A Low-Power DCO Using Interlaced Hysteresis Delay Cells. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 673-677.	3.0	22
71	A Low Voltage All-Digital On-Chip Oscillator Using Relative Reference Modeling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1615-1620.	3.1	14
72	Stochastic decoding for LDPC convolutional codes. , 2012, , .		2

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73	An Efficient DPA Countermeasure With Randomized Montgomery Operations for DF-ECC Processor. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 287-291.	3.0	22
74	Development and validation of a self-rating scale for betel quid chewers based on a male-prisoner population in Taiwan: The Betel Quid Dependence Scale. Drug and Alcohol Dependence, 2012, 121, 18-22.	3.2	51
75	A 5.79-Gb/s Energy-Efficient Multirate LDPC Codec Chip for IEEE 802.15.3c Applications. IEEE Journal of Solid-State Circuits, 2012, 47, 2246-2257.	5.4	51
76	A high-performance elliptic curve cryptographic processor over GF(p) with SPA resistance. , 2012, , .		31
77	A QPSK/16-QAM OFDM-based 29.1Mbps LINC transmitter for Body Channel Communication. , 2012, , .		6
78	A low cost DPA-resistant 8-bit AES core based on ring oscillators. , 2012, , .		0
79	A 2.37-Gb/s 284.8 mW Rate-Compatible (491,3,6) LDPC-CC Decoder. IEEE Journal of Solid-State Circuits, 2012, 47, 817-831.	5.4	14
80	A True Random-Based Differential Power Analysis Countermeasure Circuit for an AES Engine. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 103-107.	3.0	24
81	A 2.56 Gb/s soft RS (255,239) decoder chip for optical communication systems. , 2011, , .		4
82	A low power all-digital signal component separator for uneven multi-level LINC systems. , 2011, , .		4
83	An energy-efficient OFDM-based baseband transceiver design for ubiquitous healthcare monitoring applications. , 2011, , .		3
84	A 2.97 Gb/s DPA-resistant AES engine with self-generated random sequence. , 2011, , .		9
85	A dual-field elliptic curve cryptographic processor with a radix-4 unified division unit. , 2011, , .		14
86	A Low-Power and Portable Spread Spectrum Clock Generator for SoC Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1113-1117.	3.1	14
87	A Sub-mW All-Digital Signal Component Separator With Branch Mismatch Compensation for OFDM LINC Transmitters. IEEE Journal of Solid-State Circuits, 2011, 46, 2514-2523.	5.4	13
88	A Predefined Bit-Plane Comparison Coding for Mobile Video Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 437-441.	3.0	0
89	A 90Ânm All-digital Smart Temperature Sensor with Wireless Body Area Network Baseband Transceiver for Biotelemetry Applications. Journal of Signal Processing Systems, 2011, 64, 241-248.	2.1	0
90	A 0.67mW 14.55Mbps OFDM-based sensor node transmitter for body channel communications. , 2011, , .		5

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91	A low-power all-digital phase modulator pair for LINC transmitters. , 2011, , .		1
92	A Robust Frequency Tracking Loop for Energy-Efficient Crystalless WBAN Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 637-641.	3.0	4
93	A micropower biomedical signal processor for mobile healthcare applications. , 2011, , .		16
94	An area-efficient high-accuracy prediction-based CABAC decoder architecture for H.264/AVC. , 2011, , .		7
95	Fast-lock all-digital DLL and digitally-controlled phase shifter for DDR controller applications. IEICE Electronics Express, 2010, 7, 634-639.	0.8	6
96	A 26.9 K 314.5 Mb/s Soft (32400,32208) BCH Decoder Chip for DVB-S2 System. IEEE Journal of Solid-State Circuits, 2010, , .	5.4	13
97	A frequency accuracy enhanced sub-10µW on-chip clock generator for energy efficient crystal-less wireless biotelemetry applications. , 2010, , .		3
98	A low-power radix-4 Viterbi decoder based on DCVSPG pulsed latch with sharing technique. , 2010, , .		3
99	A sub-mW all-digital signal component separator with branch mismatch compensation for OFDM LINC transmitters. , 2010, , .		1
100	A Low Overhead DPA Countermeasure Circuit Based on Ring Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 546-550.	3.0	32
101	An improved soft BCH decoder with one extra error compensation. , 2010, , .		6
102	A 521-bit dual-field elliptic curve cryptographic processor with power analysis resistance. , 2010, , .		27
103	A Sub-10-$muhbox{W}$ Digitally Controlled Oscillator Based on Hysteresis Delay Cell Topologies for WBAN Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 951-955.	3.0	14
104	A Generalized Mixed-Radix Algorithm for Memory-Based FFT Processors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 26-30.	3.0	64
105	A low-power all-digital signal component separator for OFDM LINC systems. , 2010, , .		2
106	Turbo Decoder Using Contention-Free Interleaver and Parallel Architecture. IEEE Journal of Solid-State Circuits, 2010, 45, 422-432.	5.4	23
107	A 5.7Gbps row-based layered scheduling LDPC decoder for IEEE 802.15.3c applications. , 2010, , .		6
108	Design of an intra predictor with data reuse for high-profile H.264 applications. , 2009, , .		5

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109	A synchronization method for crystal-less OFDM-based wireless body area network applications. , 2009, , .		6
110	An eCrystal oscillator with self-calibration capability. , 2009, , .		8
111	A 0.92mm² 23.4mW fully-compliant CTC decoder for WiMAX 802.16e application. , 2009, , .		0
112	A Universal VLSI Architecture for Reedâ€“Solomon Error-and-Erasure Decoders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1960-1967.	5.4	6
113	A 26.9K 314.5Mbps soft (32400, 32208) BCH decoder chip for DVB-S2 system. , 2009, , .		0
114	A 1.69 Gb/s area-efficient AES crypto core with compact on-the-fly key expansion unit. , 2009, , .		16
115	A 0.5 V 4.85 Mbps Dual-Mode Baseband Transceiver With Extended Frequency Calibration for Biotelemetry Applications. IEEE Journal of Solid-State Circuits, 2009, 44, 2966-2976.	5.4	20
116	A sub-100μW area-efficient digitally-controlled oscillator based on hysteresis delay cell topologies. , 2009, , .		1
117	Design of an H.264/AVC Decoder with Memory Hierarchy and Line-Pixel-Lookahead. Journal of Signal Processing Systems, 2008, 50, 69-80.	2.1	3
118	An Indexed-Scaling Pipelined FFT Processor for OFDM-Based WPAN Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 146-150.	3.0	48
119	An LDPC Decoder Chip Based on Self-Routing Network for IEEE 802.16e Applications. IEEE Journal of Solid-State Circuits, 2008, 43, 684-694.	5.4	111
120	A 2.4-Gsample/s DVFS FFT Processor for MIMO OFDM Communication Systems. IEEE Journal of Solid-State Circuits, 2008, 43, 1260-1273.	5.4	91
121	An OFDMA-based wireless body area network using frequency pre-calibration. , 2008, , .		2
122	A 0.5V 4.85Mbps dual-mode baseband transceiver with extended frequency calibration for biotelemetry applications. , 2008, , .		0
123	Multi-mode message passing switch networks applied for QC-LDPC decoder. , 2008, , .		7
124	A Symbol-Rate Timing Synchronization Method for Low Power Wireless OFDM Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 922-926.	3.0	9
125	A Low-Power Viterbi Decoder Based on Scarce State Transition and Variable Truncation Length. , 2007, , .		3
126	A Joint Architecture of Error-Concealed Deblocking Filter for H.264/AVC Video Transmission. , 2007, , .		2

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127	An all-digital phase-frequency tunable clock generator for wireless OFDM communications systems. , 2007, , .		3
128	A Dynamic Phase-Frequency Recovery for Power Reduction in OFDM Systems. , 2007, , .		1
129	A 125 $mu{hbox{W}}$, Fully Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications. IEEE Journal of Solid-State Circuits, 2007, 42, 161-169.	5.4	72
130	An Ultra-Low-Power and Portable Digitally Controlled Oscillator for SoC Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 954-958.	3.0	71
131	Generalized MLP/BP-based MIMO DFEs for Overcoming ISI and ACI in Band-limited Channels. , 2007, , .		2
132	Design of an FFT/IFFT Processor for MIMO OFDM Systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 807-815.	0.1	111
133	A New Soft Variable Length Decoder for Wireless Video Transmission. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 224-236.	8.3	3
134	A 0.22 nJ/b/iter 0.13 μm turbo decoder chip using inter-block permutation interleaver. , 2007, , .		4
135	A Channel Equalizer Design for COFDM System. , 2006, , .		1
136	An All-Digital Delay-Locked Loop for DDR SDRAM Controller Applications. , 2006, , .		10
137	An Improved Soft-Input CAVLC Decoder for Mobile Communication Applications. , 2006, , .		0
138	A Fast-Lock-In ADPLL with High-Resolution and Low-Power DCO for SoC Applications. , 2006, , .		9
139	A Clock Generator With Cascaded Dynamic Frequency Counting Loops for Wide Multiplication Range Applications. IEEE Journal of Solid-State Circuits, 2006, 41, 1275-1285.	5.4	48
140	A Low-Complexity Synchronizer for OFDM-Based UWB System. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1269-1273.	2.2	19
141	An All-Digital Phase-Locked Loop with High-Resolution for SoC Applications. , 2006, , .		28
142	A MT-CDMA based wireless body area network for ubiquitous healthcare monitoring. , 2006, , .		7
143	A Self-Grouping and Table-Merging Algorithm for VLC-Based Video Decoding System. , 2006, , .		3
144	SoC for COFDM Wireless Communications: Challenges and Opportunities. , 2006, , .		3

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145	Memory-Hierarchy-Based Power Reduction for H. 264/AVC Video Decoder. , 2006, , .		3
146	Guest Editorial: System-on-a-Chip for Multimedia Systems. Journal of Signal Processing Systems, 2005, 41, 5-7.	1.0	0
147	An area-efficient and high-throughput de-blocking filter for multi-standard video applications. , 2005, , .		3
148	A MRMDF FFT Processor for MIMO OFDM Applications. , 2005, , .		0
149	Design of a power-reduction Viterbi decoder for WLAN applications. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 1148-1156.	0.1	54
150	An 865-Î¼W H.264/AVC Video Decoder for Mobile Applications. , 2005, , .		15
151	A 1-GS/s FFT/IFFT processor for UWB applications. IEEE Journal of Solid-State Circuits, 2005, 40, 1726-1735.	5.4	184
152	A portable digitally controlled oscillator using novel varactors. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 233-237.	2.2	90
153	A New DLL-Based Approach for All-Digital Multiphase Clock Generation. IEEE Journal of Solid-State Circuits, 2004, 39, 469-475.	5.4	53
154	A dynamic scaling FFT processor for DVB-T applications. IEEE Journal of Solid-State Circuits, 2004, 39, 2005-2013.	5.4	93
155	Two-level hierarchical Z-buffer with compression technique for 3D graphics hardware. Visual Computer, 2003, 19, 467-479.	3.5	4
156	An all-digital phase-locked loop for high-speed clock generation. IEEE Journal of Solid-State Circuits, 2003, 38, 347-351.	5.4	174
157	Error-resilient image coding (ERIC) with smart-IDCT error concealment technique for wireless multimedia transmission. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 176-181.	8.3	8
158	A Low-Power Design for Reedâ€“Solomon Decoders. Journal of Circuits, Systems and Computers, 2003, 12, 159-170.	1.5	0
159	Design of a wide-band frequency synthesizer based on TDC and DVC techniques. IEEE Journal of Solid-State Circuits, 2002, 37, 1244-1255.	5.4	4
160	A Reed-Solomon product-code (RS-PC) decoder chip for DVD applications. IEEE Journal of Solid-State Circuits, 2001, 36, 229-238.	5.4	49
161	A new approach of group-based VLC codec system with full table programmability. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 210-221.	8.3	39
162	Design and analysis of a portable high-speed clock generator. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 367-375.	2.2	33

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163	A cost effective lighting processor for 3D graphics application. , 1999, , .		3
164	An efficient VLSI architecture for separable 2-D discrete wavelet transform. , 1999, , .		4
165	A generalized prediction method for modified memory-based high throughput VLC decoder design. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1999, 46, 742-754.	2.2	7
166	A new anti-aliasing algorithm for computer graphics images. , 1999, , .		2
167	An efficient VLC decompression scheme for user-defined coding tables. , 1999, , .		1
168	An Area Efficient Architecture For 3d Graphics Shading *. , 1998, , .		0
169	A multicasting solution for ATM video applications. IEEE Transactions on Circuits and Systems for Video Technology, 1997, 7, 675-686.	8.3	2
170	An Efficient VLSI Architecture for Full-Search Block Matching Algorithms. Journal of Signal Processing Systems, 1997, 15, 275-282.	1.0	7
171	Finite state vector quantization with multipath tree search strategy for image/video coding. IEEE Transactions on Circuits and Systems for Video Technology, 1996, 6, 287-294.	8.3	6
172	A wideband digital frequency synthesizer. , 0, , .		0
173	An efficient modeling codec architecture for binary shape coding. , 0, , .		1
174	An Area-efficient Median Filtering IC For Image/video Applications. , 0, , .		0
175	An efficient memory architecture for motion estimation processor design. , 0, , .		8
176	Semi-systolic array based motion estimation processor design. , 0, , .		4
177	A cost-effective VLSI architecture for high-throughput sequential decoder. , 0, , .		2
178	A memory-based architecture for very-high-throughput variable length codec design. , 0, , .		7
179	Effects of shadowing, multipath fading, antenna diversity in DS/CDMA for cellular mobile radio with reverse-link power control. , 0, , .		0
180	A multicasting solution for ATM video applications. , 0, , .		0

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181	Buffer size optimization for full-search block matching algorithms. , 0, , .		0
182	Construction of error resilient synchronization codeword for variable-length code in image transmission. , 0, , .		1
183	A 1.5-V, 2.4GHz CMOS low-noise amplifier. , 0, , .		3
184	A new approach of group-based VLC codec system. , 0, , .		2
185	A high clock-offset tolerance for DSSS synchronization. , 0, , .		0
186	A line-based, memory efficient and programmable architecture for 2D DWT using lifting scheme. , 0, , .		22
187	A novel subcircuit extraction algorithm by recursive identification scheme. , 0, , .		6
188	A 1.75 GHz inductor-less CMOS low noise amplifier with high-Q active inductor load. , 0, , .		4
189	A novel single-bit input all digital synchronizer and demodulator baseband processor for fast frequency hopping system. , 0, , .		2
190	An area-efficient architecture for Reed-Solomon decoder using the inversionless decomposed Euclidean algorithm. , 0, , .		6
191	A novel structure for portable digitally controlled oscillator. , 0, , .		7
192	A novel fixed bit plane error resilient image coding for wireless multimedia transmission. , 0, , .		0
193	FPGA education and research activities in Taiwan. , 0, , .		3
194	A novel DCT-based bit plane error resilient entropy coding scheme and codec for wireless image communication. , 0, , .		0
195	An all-digital phase-locked loop for high-speed clock generation. , 0, , .		1
196	A high throughput low cost context-based adaptive arithmetic codec for multiple standards. , 0, , .		13
197	A high throughput context-based adaptive arithmetic codec for JPEG2000. , 0, , .		11
198	A low-power Reed-Solomon decoder for STM-16 optical communications. , 0, , .		18

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199	A design of CMOS broadband amplifier with high-Q active inductor. , 0, , .		4
200	A low power and high speed Viterbi decoder chip for WLAN applications. , 0, , .		7
201	Combining adaptive smoothing and decision-directed channel estimation schemes for OFDM WLAN systems. , 0, , .		1
202	A power and area efficient multi-mode FEC processor. , 0, , .		0
203	An universal VLSI architecture for bit-parallel computation in GF(2/sup m/). , 0, , .		6
204	A dual mode channel decoder for 3GPP2 mobile wireless communications. , 0, , .		1
205	A low-complexity soft vlc decoder using performance modeling. , 0, , .		1
206	A COFDM baseband processor with robust synchronization for high-speed WLAN applications. , 0, , .		1
207	Memory efficient and low complexity scalable soft VLC decoding for the video transmission. , 0, , .		2
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