Wim Dehaene

List of Publications by Year
in descending order

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108	2,832	186265	197818
papers	citations	28 h-index	49 g-index

109	109	109	2588
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design Margin Reduction Through Completion Detection in a 28-nm Near-Threshold DSP Processor. IEEE Journal of Solid-State Circuits, 2022, 57, 651-660.	5.4	8
2	SRAM With Stability Monitoring and Body Bias Tuning for Biomedical Applications. IEEE Solid-State Circuits Letters, 2022, 5, 29-32.	2.0	1
3	Positive-Feedback-Based Design Technique for Inherently Stable Active Load Toward High-Gain Amplifiers With Unipolar a-IGZO TFT Devices. IEEE Solid-State Circuits Letters, 2022, 5, 37-40.	2.0	3
4	External compensation for highâ€resolution active matrix organic lightâ€emitting diode displays. Journal of the Society for Information Display, 2021, 29, 511-525.	2.1	5
5	OxRRAM-Based Analog in-Memory Computing for Deep Neural Network Inference: A Conductance Variability Study. IEEE Transactions on Electron Devices, 2021, 68, 2301-2305.	3.0	10
6	A Comprehensive Study of Nanosheet and Forksheet SRAM for Beyond N5 Node. IEEE Transactions on Electron Devices, 2021, 68, 3819-3825.	3.0	26
7	The Complementary FET (CFET) 6T-SRAM. IEEE Transactions on Electron Devices, 2021, 68, 6106-6111.	3.0	12
8	A 5-GS/s 7.2-ENOB Time-Interleaved VCO-Based ADC Achieving 30.5 fJ/cs. IEEE Journal of Solid-State Circuits, 2020, , 1-11.	5.4	28
9	Bridging the Gap between Secondary and Higher STEM Education â€“ the Case of STEM@school. European Review, 2020, 28, S135-S157.	0.7	9
10	Completion Detection-Based Timing Error Detection and Correction in a Near-Threshold RISC-V Microprocessor in FDSOI 28 nm. IEEE Solid-State Circuits Letters, 2020, 3, 230-233.	2.0	7
11	Teachersâ€™ Attitudes Toward Teaching Integrated STEM: the Impact of Personal Background Characteristics and School Context. International Journal of Science and Mathematics Education, 2019, 17, 987-1007.	2.5	29
12	Crossover Logic: A Low-Power Topology for Unipolar Dual-Gate Thin-Film Technologies. IEEE Solid-State Circuits Letters, 2019, 2, 49-52.	2.0	8
13	Performance Comparison of s-Si, In0.53Ga0.47As, Monolayer BP- and WS2-Based n-MOSFETs for Future Technology Nodesâ€”Part II: Circuit-Level Comparison. IEEE Transactions on Electron Devices, 2019, 66, 3614-3619.	3.0	0
14	Integration of highly crystalline C8-BTBT thin-films into simple logic gates and circuits. Organic Electronics, 2019, 67, 64-71.	2.6	20
15	Introduction to the Special Issue on the 2018 International Solid-State Circuits Conference (ISSCC). IEEE Journal of Solid-State Circuits, 2019, 54, 3-5.	5.4	0
16	Sense amplifier offset voltage analysis for both time-zero and time-dependent variability. Microelectronics Reliability, 2019, 99, 52-61.	1.7	1
17	Performance Comparison of s-Si, In_{0.53}Ga_{0.47}As, Monolayer BP, and WS₂-Based n-MOSFETs for Future Technology Nodesâ€”Part I: Device-Level Comparison. IEEE Transactions on Electron Devices, 2019, 66, 3608-3613.	3.0	3
18	Ultrasound In-Body Communication with OFDM through Multipath Realistic Channels. , 2019, , .		13

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19	Enabling Ultrasound In-Body Communication: FIR Channel Models and QAM Experiments. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 135-144.	4.0	24
20	The influence of teachersâ€™ attitudes and school context on instructional practices in integrated STEM education. Teaching and Teacher Education, 2018, 71, 190-205.	3.2	89
21	Material-Device-Circuit Co-Design of 2-D Materials-Based Lateral Tunnel FETs. IEEE Journal of the Electron Devices Society, 2018, 6, 979-986.	2.1	8
22	How school context and personal factors relate to teachersâ€™ attitudes toward teaching integrated STEM. International Journal of Technology and Design Education, 2018, 28, 631-651.	2.6	40
23	Modelling of Channels for Intra-Corporal Ultrasound Communication. , 2018, , .		2
24	A sub 10 pJ/Cycle Over a 2 to 200 MHz Performance Range RISC- V Microprocessor in 28 nm FDSOI. , 2018, , .		10
25	Analytic variability study of inference accuracy in RRAM arrays with a binary tree winner-take-all circuit for neuromorphic applications. , 2018, , .		4
26	Margin Elimination Through Timing Error Detection in a Near-Threshold Enabled 32-bit Microcontroller in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2101-2113.	5.4	27
27	STEM Education in Flanders: How STEM@school Aims to Foster STEM Literacy and a Positive Attitude towards STEM. IEEE Instrumentation and Measurement Magazine, 2018, 21, 36-40.	1.6	21
28	Toward Temperature Tracking With Unipolar Metal-Oxide Thin-Film SAR C-2C ADC on Plastic. IEEE Journal of Solid-State Circuits, 2018, 53, 2263-2272.	5.4	42
29	Impact and mitigation of SRAM read path aging. Microelectronics Reliability, 2018, 87, 158-167.	1.7	4
30	Architecture optimization for energy-efficient resolution-scalable 8â€“12-bit SAR ADCs. Analog Integrated Circuits and Signal Processing, 2018, 97, 437-448.	1.4	4
31	Tackling misconceptions in geometrical optics. Physics Education, 2018, 53, 045020.	0.5	13
32	Power saving through state retention in IGZO-TFT AMOLED displays for wearable applications. Journal of the Society for Information Display, 2017, 25, 222-228.	2.1	44
33	A Differential Transmission Gate Design Flow for Minimum Energy Sub-10-pJ/Cycle ARM Cortex-M0 MCUs. IEEE Journal of Solid-State Circuits, 2017, 52, 1904-1914.	5.4	38
34	DVAFS: Trading computational accuracy for energy through dynamic-voltage-accuracy-frequency-scaling. , 2017, , .		30
35	High-speed single cable synchronization system for data-converters. Analog Integrated Circuits and Signal Processing, 2017, 90, 283-290.	1.4	0
36	Introduction to the Special Issue on the 46th European Solid-State Circuits Conference (ESSCIRC). IEEE Journal of Solid-State Circuits, 2017, 52, 1700-1702.	5.4	0

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37	A Thin-Film, a-IGZO, 128b SRAM and LPROM Matrix With Integrated Periphery on Flexible Foil. IEEE Journal of Solid-State Circuits, 2017, 52, 3095-3103.	5.4	19
38	Material-Device-Circuit Co-optimization of 2D Material based FETs for Ultra-Scaled Technology Nodes. Scientific Reports, 2017, 7, 5016.	3.3	16
39	Device circuit and technology co-optimisation for FinFET based 6T SRAM cells beyond N7. , 2017, , .		5
40	A 16.07pJ/cycle 31MHz fully differential transmission gate logic ARM Cortex M0 core in 40nm CMOS. , 2016, , .		10
41	Fineâ€grained hardware switching scheme for power reduction in multiplication. Electronics Letters, 2016, 52, 1374-1375.	1.0	0
42	A mm-Precise 60 GHz Transmitter in 40 nm CMOS for Discrete-Carrier Indoor Localization. IEEE Journal of Solid-State Circuits, 2015, 50, 1604-1617.	5.4	12
43	Benchmarking of MoS₂FETs With Multigate Si-FET Options for 5 nm and Beyond. IEEE Transactions on Electron Devices, 2015, 62, 4051-4056.	3.0	29
44	Development of an Ultralow-Power Injection-Locked PSK Receiver Architecture. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 31-35.	3.0	2
45	Impact analysis of deep-submicron CMOS technologies on the voltage and temperature independence of a time-domain sensor interface. Analog Integrated Circuits and Signal Processing, 2015, 82, 285-296.	1.4	1
46	On the effect of technology scaling on variation-resilient sub-threshold circuits. Solid-State Electronics, 2015, 103, 19-29.	1.4	6
47	Accounting for variability in the design of circuits with organic thin-film transistors. Organic Electronics, 2014, 15, 937-942.	2.6	17
48	Low-Power Digital Signal Processor Architecture for Wireless Sensor Nodes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 313-321.	3.1	24
49	An MLS-Prony implementation for a cm-Precise Super 10 m range 802.15.3c-PHY 60ÂGHz positioning application. Journal of Ambient Intelligence and Humanized Computing, 2014, 5, 623-634.	4.9	4
50	Bidirectional Communication in an HF Hybrid Organic/Solution-Processed Metal-Oxide RFID Tag. IEEE Transactions on Electron Devices, 2014, 61, 2387-2393.	3.0	27
51	Design of a frequency reference based on a PVT-independent transmission line delay. , 2014, , .		0
52	A remotely-powered, 20ÂMb/s, 5.35ÂpJ/bit impulse-UWB WSN tag for cm-accurate-localization sensor networks. Analog Integrated Circuits and Signal Processing, 2014, 80, 531-540.	1.4	1
53	Transient Behavior and Phase Noise Performance of Pulsed-Harmonic Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2119-2128.	5.4	2
54	Joint Estimation of Propagation Delay Dispersion and Time of Arrival in a 40-nm CMOS Comparator Bank for Time-Based Receivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 76-80.	3.0	2

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55	Teaching HW/SW Co-Design With a Public Key Cryptography Application. IEEE Transactions on Education, 2013, 56, 478-483.	2.4	9
56	Presilicon Circuit-Aware Linear Least Squares Spectral Analysis for Time-Based Data Converters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 751-755.	3.0	2
57	Developing engineering-oriented educational workshops within a student branch. , 2013, , .		0
58	Optimized circuit design for flexible 8-bit RFID transponders with active layer of ink-jet printed small molecule semiconductors. Organic Electronics, 2013, 14, 768-774.	2.6	70
59	Supply-Noise-Resilient Design of a BBPLL-Based Force-Balanced Wheatstone Bridge Interface in 130-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2618-2627.	5.4	52
60	Development of an open-source smart energy house for K-12 education. , 2013, , .		3
61	Extending dynamic range of RF PWM transmitters. Electronics Letters, 2013, 49, 430-432.	1.0	11
62	Wobble-based on-chip calibration circuit for temperature independent oscillators. Electronics Letters, 2012, 48, 1000-1001.	1.0	2
63	Ultra Low-Energy SRAM Design for Smart Ubiquitous Sensors. IEEE Micro, 2012, 32, 10-24.	1.8	15
64	A Fully Digital Delay Line Based GHz Range Multimode Transmitter Front-End in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 1681-1692.	5.4	53
65	A 65 nm, 850 MHz, 256 kbit, 4.3 pJ/access, Ultra Low Leakage Power Memory Using Dynamic Cell Stability and a Dual Swing Data Link. IEEE Journal of Solid-State Circuits, 2012, 47, 1784-1796.	5.4	15
66	A Novel, Highly Linear, Voltage and Temperature Independent Sensor Interface using Pulse Width Modulation. Procedia Engineering, 2012, 47, 1215-1218.	1.2	8
67	Complementary integrated circuits on plastic foil using inkjet printed n- and p-type organic semiconductors: Fabrication, characterization, and circuit analysis. Organic Electronics, 2012, 13, 1686-1692.	2.6	54
68	A low leakage 500MHz 2T embedded dynamic memory with integrated semi-transparent refresh. Solid-State Electronics, 2012, 75, 55-62.	1.4	1
69	Linking EUV lithography line edge roughness and 16nm NAND memory performance. Microelectronic Engineering, 2012, 98, 24-28.	2.4	12
70	Test Structures for Characterization of Through-Silicon Vias. IEEE Transactions on Semiconductor Manufacturing, 2012, 25, 355-364.	1.7	23
71	A CMOS Burst-Mode Transmitter With Watt-Level RF PA and Flexible Fully Digital Front-End. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 613-617.	3.0	25
72	Variation-Resilient Building Blocks for Ultra-Low-Energy Sub-Threshold Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 898-902.	3.0	15

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73	An Ultra-Low-Power, Batteryless Microsystem for Wireless Sensor Networks. Procedia Engineering, 2012, 47, 1406-1409.	1.2	1
74	Trades-off between lithography line edge roughness and error-correcting codes requirements for NAND Flash memories. Microelectronics Reliability, 2012, 52, 525-529.	1.7	2
75	Technology Assessment of Through-Silicon Via by Using Câ€“V and Câ€“t Measurements. IEEE Electron Device Letters, 2011, 32, 946-948.	3.9	15
76	Multiple Event Time-to-Digital Conversion-Based Pulse Digitization for a 250 MHz Pulse Radio Ranging Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2614-2622.	5.4	7
77	Unipolar Organic Transistor Circuits Made Robust by Dual-Gate Technology. IEEE Journal of Solid-State Circuits, 2011, 46, 1223-1230.	5.4	114
78	A 4.4 pJ/Access 80 MHz, 128 kbit Variability Resilient SRAM With Multi-Sized Sense Amplifier Redundancy. IEEE Journal of Solid-State Circuits, 2011, 46, 2416-2430.	5.4	26
79	A novel, PLL-based frequency-to-digital conversion mechanism for sensor interfaces. Sensors and Actuators A: Physical, 2011, 172, 220-227.	4.1	22
80	A Synchronization-Free Spread Spectrum Clock Generation Technique for Automotive Applications. IEEE Transactions on Electromagnetic Compatibility, 2011, 53, 169-177.	2.2	6
81	Cross-cell interference variability aware model of fully planar NAND Flash memory including line edge roughness. Microelectronics Reliability, 2011, 51, 919-924.	1.7	31
82	Integration challenges of copper Through Silicon Via (TSV) metallization for 3D-stacked IC integration. Microelectronic Engineering, 2011, 88, 745-748.	2.4	66
83	Temperature-Dependent Modeling and Characterization of Through-Silicon Via Capacitance. IEEE Electron Device Letters, 2011, 32, 563-565.	3.9	42
84	Organic RFID transponder chip with data rate compatible with electronic product coding. Organic Electronics, 2010, 11, 1176-1179.	2.6	237
85	(Invited) Towards EPC Compatible Plastic RFID Tags. ECS Transactions, 2010, 33, 383-389.	0.5	4
86	A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2404-2412.	5.4	65
87	Circuit Design for Bias Compatibility in Novel FinFET-Based Floating-Body RAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 183-187.	3.0	0
88	Through-Silicon-Via Capacitance Reduction Technique to Benefit 3-D IC Performance. IEEE Electron Device Letters, 2010, 31, 549-551.	3.9	78
89	Plastic circuits and tags for 13.56MHz radio-frequency communication. Solid-State Electronics, 2009, 53, 1220-1226.	1.4	127
90	A 3-tier UWB-based indoor localization system for ultra-low-power sensor networks. IEEE Transactions on Wireless Communications, 2009, 8, 2813-2818.	9.2	30

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91	Performance analysis of a flexible subsampling receiver for pulsed UWB signals. IEEE Transactions on Wireless Communications, 2009, 8, 4134-4142.	9.2	7
92	A 3.6 pJ/Access 480 MHz, 128 kb On-Chip SRAM With 850 MHz Boost Mode in 90 nm CMOS With Tunable Sense Amplifiers. IEEE Journal of Solid-State Circuits, 2009, 44, 2065-2077.	5.4	39
93	UML for electronic systems design: a comprehensive overview. Design Automation for Embedded Systems, 2008, 12, 261-292.	1.0	54
94	A high speed, low voltage to high voltage level shifter in standard 1.2ÂV 0.13ÂÎ¼m CMOS. Analog Integrated Circuits and Signal Processing, 2008, 55, 85-91.	1.4	15
95	Analysis of the QAC IR-UWB Receiver for Low Energy, Low Data-Rate Communication. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2423-2432.	5.4	13
96	A Flexible, Ultra-Low-Energy 35 pJ/Pulse Digital Back-End for a QAC IR-UWB Receiver. IEEE Journal of Solid-State Circuits, 2008, 43, 1677-1687.	5.4	10
97	Impact of Random Soft Oxide Breakdown on SRAM Energy/Delay Drift. IEEE Transactions on Device and Materials Reliability, 2007, 7, 581-591.	2.0	26
98	A Low-Power Embedded SRAM for Wireless Applications. IEEE Journal of Solid-State Circuits, 2007, 42, 1607-1617.	5.4	31
99	A CMOS Ultra-Wideband Receiver for Low Data-Rate Communication. IEEE Journal of Solid-State Circuits, 2007, 42, 2515-2527.	5.4	63
100	SmartMIMO: Energy-Aware Adaptive MIMO-OFDM Radio Link Control for Wireless Local Area Networks. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2006, , .	0.0	5
101	Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies. IEEE Journal of Solid-State Circuits, 2006, 41, 2577-2588.	5.4	365
102	Cross-layer power management in wireless networks and consequences on system-level architecture. Signal Processing, 2006, 86, 1792-1803.	3.7	12
103	A small granular controlled leakage reduction system for SRAMs. Solid-State Electronics, 2005, 49, 1776-1782.	1.4	18
104	A high-voltage output driver in a 2.5-V 0.25-/spl mu/m CMOS technology. IEEE Journal of Solid-State Circuits, 2005, 40, 576-583.	5.4	71
105	Variable tapered pareto buffer design and implementation allowing run-time configuration for low-power embedded SRAMs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 1127-1135.	3.1	25
106	A 50-MHz standard CMOS pulse equalizer for hard disk read channels. IEEE Journal of Solid-State Circuits, 1997, 32, 977-988.	5.4	34
107	A CMOS rectifier-integrator for amplitude detection in hard disk servo loops. IEEE Journal of Solid-State Circuits, 1995, 30, 743-751.	5.4	39
108	Full CMOS continuous time filters for GSM applications. Annales Des Telecommunications/Annals of Telecommunications, 1993, 48, 224-232.	2.5	2