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List of Publications by Year in descending order

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1478505 1281871 17 115 11 6 citations h-index g-index papers 17 17 17 100 docs citations times ranked citing authors all docs

| # | Article | IF | CITATIONS |
|----|---|-----|-----------|
| 1 | Linear Response Modeling of High Luminous Flux Phosphor-Coated White LEDs for VLC. Journal of Lightwave Technology, 2022, 40, 3761-3767. | 4.6 | 6 |
| 2 | On the Performance and Power Consumption of Bias-T Based Drivers for High Speed VLC. Journal of Lightwave Technology, 2022, 40, 6078-6086. | 4.6 | 3 |
| 3 | Helping Pregraduate Students Reach Deep Understanding of the Second Law of Thermodynamics. Education Sciences, 2021, 11, 539. | 2.6 | 2 |
| 4 | Low Complexity System on Chip Design to Acquire Signals from MOS Gas Sensor Applications. Sensors, 2021, 21, 6552. | 3.8 | 2 |
| 5 | A Test Vector Generation Method Based on Symbol Error Probabilities for Low-Complexity Chase Soft-Decision Reed–Solomon Decoding. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2198-2207. | 5.4 | 5 |
| 6 | Soft-Decision Low-Complexity Chase Decoders for the RS(255,239) Code. Electronics (Switzerland), 2019, 8, 10. | 3.1 | 5 |
| 7 | Optimised CORDICâ€based atan2 computation for FPGA implementations. Electronics Letters, 2017, 53, 1296-1298. | 1.0 | 6 |
| 8 | Reduced-Complexity Nonbinary LDPC Decoder for High-Order Galois Fields Based on Trellis Min–Max Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2643-2653. | 3.1 | 28 |
| 9 | High-Performance NB-LDPC Decoder With Reduction of Message Exchange. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1950-1961. | 3.1 | 17 |
| 10 | Nonbinary LDPC Decoder Based on Simplified Enhanced Generalized Bit-Flipping Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1455-1459. | 3.1 | 4 |
| 11 | Serial Symbol-Reliability Based Algorithm for Decoding Non-Binary LDPC Codes. IEEE Communications Letters, 2012, 16, 909-912. | 4.1 | 9 |
| 12 | Decoder for an enhanced serial generalized bit flipping algorithm. , 2012, , . | | 4 |
| 13 | Low Complexity Time Synchronization Algorithm for OFDM Systems with Repetitive Preambles. Journal of Signal Processing Systems, 2012, 68, 287-301. | 2.1 | 5 |
| 14 | FPGA implementation of an OFDM-based WLAN receiver. Microprocessors and Microsystems, 2012, 36, 232-244. | 2.8 | 17 |
| 15 | Improved Sliced Message Passing Architecture for High Throughput Decoding of LDPC Codes. Journal of Signal Processing Systems, 2012, 66, 99-104. | 2.1 | 2 |
| 16 | POWER CONSUMPTION REDUCTION IN A VITERBI DECODER FOR OFDM-WLAN. Journal of Circuits, Systems and Computers, 2009, 18, 1333-1337. | 1.5 | 0 |
| 17 | Reduction of power consumption in a Viterbi Decoder for OFDM-WLAN., 2007,,. | | O |