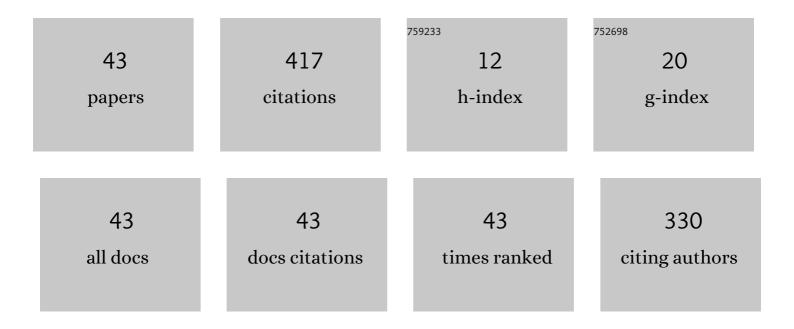
## Hiroshi Watanabe

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	How can chip technology realize electronic sensing of viruses?. , 2021, , .		0
2	Impact on the Conductance Method of the Asymmetry in the AC Response Induced by Interface Trap Levels. ECS Journal of Solid State Science and Technology, 2021, 10, 043004.	1.8	0
3	Trap-Related Reliability Problems of Dielectrics in Memory Cells. Electronics (Switzerland), 2021, 10, 1287.	3.1	1
4	Proof of Authenticity of Logistics Information with Passive RFID Tags and Blockchain. , 2021, , .		6
5	Efficient Sensing Properties of Aluminum Nitride Nanosheets toward Toxic Pollutants under Gated Electric Field. ACS Applied Electronic Materials, 2020, 2, 1645-1652.	4.3	15
6	Experimental Study of 1/f <sup>1+α</sup> Noise in Transient Leakage Current of Metal–Insulator–Metal With Stacked High-k Polycrystalline Films. IEEE Transactions on Electron Devices, 2020, 67, 2503-2509.	3.0	3
7	Graphene-Based Ultrasensitive Strain Sensors. ACS Applied Electronic Materials, 2020, 2, 523-528.	4.3	11
8	Monte Carlo simulation of random dopant fluctuation in <i>C</i> – <i>V</i> characteristics using image charge model and adequately determined length scale. Japanese Journal of Applied Physics, 2019, 58, 091004.	1.5	0
9	A Novel Chip-Level Blockchain Security Solution for the Internet of Things Networks. Technologies, 2019, 7, 28.	5.1	15
10	Monte Carlo Simulation of Nanowires Array Biosensor With AC Electroosmosis. IEEE Transactions on Electron Devices, 2018, 65, 1932-1938.	3.0	2
11	Physics of Discrete Impurities under the Framework of Device Simulations for Nanostructure Devices. Materials, 2018, 11, 2559.	2.9	12
12	Three-dimensional device simulation of random telegraph noise spectroscopy with Coulomb energy variation of the trap in high-k gate oxide. Japanese Journal of Applied Physics, 2018, 57, 124301.	1.5	1
13	Localized Tunneling Phenomena of Nanometer Scaled High- \${K}\$ Gate-Stack. IEEE Transactions on Electron Devices, 2017, 64, 3077-3083.	3.0	5
14	Monte-Carlo simulation of biomolecules' fluid-dynamics in electrolyte facing nanowires biosensor. , 2017, , .		2
15	Nano-meter scaled gate area high-K dielectrics with trap-assisted tunneling and random telegraph noise. , 2014, , .		0
16	Numerical Study of Very Small Floating Islands. IEEE Transactions on Electron Devices, 2014, 61, 1145-1152.	3.0	6
17	(Invited) Analysis of the Scaling Effect on NAND Flash Memory Cell Operation. ECS Transactions, 2013, 50, 27-35.	0.5	0
18	Integrated Batteryless Electron Timer. IEEE Transactions on Electron Devices, 2011, 58, 792-797.	3.0	1

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#	Article	IF	CITATIONS
19	Quantitative Discussion on Electron-Hole Universal Tunnel Mass in Ultrathin Dielectric of Oxide and Oxide-Nitride. ECS Transactions, 2011, 35, 303-320.	0.5	1
20	Universal Tunnel Mass and Charge Trapping in \$[( hbox{SiO}_{2})_{1-x} (hbox{Si}_{3}hbox{N}_{4})_{x}]_{1-y}hbox{Si}_{y}\$ Film. IEEE Transactions on Electron Devices, 2010, 57, 1129-1136.	3.0	8
21	Transient Device Simulation of Floating Gate Nonvolatile Memory Cell With a Local Trap. IEEE Transactions on Electron Devices, 2010, 57, 1873-1882.	3.0	6
22	A Tight Binding Method Study of Optimized \$hbox{Si}{-} hbox{SiO}_{2}\$ System. IEEE Transactions on Electron Devices, 2010, 57, 3084-3091.	3.0	4
23	Statistical simulation of metal-gate work-function fluctuation in high-κ/metal-gate devices. , 2010, , .		5
24	Depletion-Type Cell-Transistor on Partial Silicon-on-Insulator Substrate for 2× nm Generation Floating-Gate NAND Electrically Erasable Programmable Read Only Memory. Japanese Journal of Applied Physics, 2010, 49, 04DD09.	1.5	0
25	Trial Application of Tight-Binding Method to Si-Cluster Surrounded by SiO2 in Optimized Atomistic Network: Si-Cluster Surrounded SiO2 is Quite Unique. , 2009, , .		Ο
26	Transient device simulation of trap-assisted leakage in non-volatile memory cell. , 2008, , .		1
27	Numerical Study of \$C\$–\$V\$ Characteristics of Double-Gate Ultrathin SOI MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 52-58.	3.0	6
28	Statistics of Grain Boundaries in Polysilicon. IEEE Transactions on Electron Devices, 2007, 54, 38-44.	3.0	13
29	Hopping Transport of Electrons via Si-Dot. , 2007, , 249-252.		5
30	Determination of tunnel mass and physical thickness of gate oxide including poly-Si/SiO/sub 2/ and Si/SiO/sub 2/ interfacial transition Layers. IEEE Transactions on Electron Devices, 2006, 53, 1323-1330.	3.0	24
31	Leakage mechanism of ultrathin SiON gate dielectric. , 2006, , .		1
32	Numerical Study of Data Retention Due to Direct Tunneling for Nonvolatile Memory Cell. IEEE Transactions on Electron Devices, 2005, 52, 955-961.	3.0	3
33	Depletion Layer of Gate Poly-Si. IEEE Transactions on Electron Devices, 2005, 52, 2265-2271.	3.0	13
34	Reduction of Accumulation Thickness in Metal Gate. , 2005, , .		6
35	Scaling effects on gate leakage current. IEEE Transactions on Electron Devices, 2003, 50, 1779-1784.	3.0	17
36	Effects of incomplete ionization of impurities in poly-Si gate and band gap narrowing on direct tunneling gate leakage current. Journal of Applied Physics, 2001, 90, 1600-1607.	2.5	75

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#	Article	IF	CITATIONS
37	Impact of Two-Dimensional Structure of nMOSFETs on Direct Tunnel Gate Current. , 2001, , .		Ο
38	Model of Photoinduced Disaccommodation in Oxygen-deficient Yttrium Iron Garnet. Journal of the Magnetics Society of Japan, 1999, 23, 376-378.	0.4	0
39	Hidden order and symmetry breaking in the ground state of a spin-1/2 antiferromagnetic Heisenberg ladder. Physical Review B, 1995, 52, 12508-12511.	3.2	16
40	Numerical diagonalization study of anS=1/2 ladder model with open boundary conditions. Physical Review B, 1994, 50, 13442-13448.	3.2	29
41	S=1/2 Quantum Heisenberg Ladder andS=1 Haldane Phase. Journal of the Physical Society of Japan, 1993, 62, 2845-2860.	1.6	56
42	Nonlocal Unitary Transformation and Haldane State inS=1/2 Antiferromagnetic Ladder Model. Journal of the Physical Society of Japan, 1992, 61, 39-42.	1.6	27
43	Positron Lifetime in C60/C70Powder. Journal of the Physical Society of Japan, 1991, 60, 2812-2814.	1.6	21