Ashish Raman

List of Publications by Year
in descending order

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		759233	677142
54	637	12	22
papers	citations	h-index	g-index

55	55	55	234
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design and Analysis of Gate Overlapped/Underlapped NWFET Based Lable Free Biosensor. Silicon, 2022, 14, 989-996.	3.3	1
2	Design of Dopingless GaN Nanowire FET with Low â€˜Qâ€™ for High Switching and RF Applications. Silicon, 2022, 14, 1297-1307.	3.3	7
3	Overlapped Gate-Source/Drain H-shaped TFET: Proposal, Design and Linearity Analysis. Silicon, 2022, 14, 6415-6424.	3.3	3
4	Human-Machine Interface-Based Robotic Wheel Chair Control. Advances in Medical Technologies and Clinical Practice Book Series, 2022, , 1-22.	0.3	0
5	CuO/Pentacene Type-II Planar Heterojunction for UV-Vis-NIR Photodetection With High EQE. IEEE Transactions on Electron Devices, 2022, 69, 722-728.	3.0	2
6	Design and investigation of field plate-based vertical GAA â€“ Î²-(AlGa)2O3/Ga2O3 high electron mobility transistor. Superlattices and Microstructures, 2022, 164, 107117.	3.1	3
7	Electrostatic-Doped Nanotube TFET: Proposal, Design, and Investigation with Linearity Analysis. Silicon, 2021, 13, 2401-2413.	3.3	8
8	Novel Vertical GAA-AlGaN/GaN Dopingless MIS-HEMT: Proposal and Investigation. Transactions on Electrical and Electronic Materials, 2021, 22, 473-480.	1.9	0
9	A charge-based capacitance model for double-gate hetero-gate-dielectric tunnel FET. Superlattices and Microstructures, 2021, 150, 106748.	3.1	3
10	Novel Asymmetric Recessed-Gate/Source Architecture Advancement of Dual-Metal-Gate SiGe/Si Dopingless Nanowire-TFET for Low-Voltage Performance Optimization. Silicon, 2021, 13, 3141-3151.	3.3	4
11	Charge-Plasma Based Cylindrical Nanowire FET for Low-Noise and High Sensing. ECS Journal of Solid State Science and Technology, 2021, 10, 021003.	1.8	5
12	Design, Investigation, and Sensitivity Analysis of a Biosensor Based on an Optimized Electrostatically Doped Nanotube TFET. Journal of Electronic Materials, 2021, 50, 5462-5471.	2.2	3
13	Tweaking the Performance of Dopingless Nano-TFET with Misaligned Sandwiched Dual-Gate Structure. Silicon, 2021, 13, 3713-3723.	3.3	2
14	Low voltage charge-plasma based dopingless Tunnel Field Effect Transistor: analysis and optimization. Microsystem Technologies, 2020, 26, 1343-1350.	2.0	25
15	Spectroscopic and Simulation Analysis of Facile PEDOT:PSS Layer Deposition-Silicon for Perovskite Solar Cell. Silicon, 2020, 12, 1769-1777.	3.3	7
16	Design and Analog Performance Analysis of Charge-Plasma Based Cylindrical GAA Silicon Nanowire Tunnel Field Effect Transistor. Silicon, 2020, 12, 2627-2634.	3.3	15
17	Design and Investigation of Pressure Sensor Based on Charge Plasma Silicon NWFET with Cylindrical Gate Diaphragm. Silicon, 2020, 12, 2479-2487.	3.3	6
18	Cylindrical Nanowire-TFET with Core-Shell Channel Architecture: Design and Investigation. Silicon, 2020, 12, 2329-2336.	3.3	13

#	Article	IF	Citations
19	Prospective Sensing Applications of Novel Heteromaterial Based Dopingless Nanowire-TFET at Low Operating Voltage. IEEE Nanotechnology Magazine, 2020, 19, 527-534.	2.0	27
20	Design and optimization of junctionless-based devices with noise reduction for ultra-high frequency applications. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	9
21	Performance Tuning and Reliability Analysis of the Electrostatically Configured Nanotube Tunnel FET with Impact of Interface Trap Charges. Silicon, 2020, , 1.	3.3	2
22	Performance analysis of electrostatic plasma-based dopingless nanotube TFET. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	15
23	An explicit surface potential, capacitance and drain current model for double-gate TFET. Superlattices and Microstructures, 2020, 140, 106431.	3.1	10
24	High-performance dual-gate-charge-plasma-AlGaN/GaN MIS-HEMT. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	14
25	Design and analysis of dual-gate misalignment on the performance of dopingless tunnel field effect transistor. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	11
26	Charge-Plasma-Based Negative Capacitance Ring-FET: Design, Investigation and Reliability Analysis. Journal of Electronic Materials, 2020, 49, 4852-4863.	2.2	12
27	Novel Design Approach of Extended Gate-On-Source Based Charge-Plasma Vertical-Nanowire TFET: Proposal and Extensive Analysis. IEEE Nanotechnology Magazine, 2020, 19, 421-428.	2.0	25
28	Distance Based Enhanced Threshold Sensitive Stable Election Routing Protocol for Heterogeneous Wireless Sensor Network. Studies in Computational Intelligence, 2019, , 101-122.	0.9	10
29	Design and Investigation of a Novel Charge Plasma-Based Core-Shell Ring-TFET: Analog and Linearity Analysis. IEEE Transactions on Electron Devices, 2019, 66, 3506-3512.	3.0	49
30	Design and Analysis of Novel Charge-Plasma Based Dopingless U-Shaped FET. , 2019, , .		1
31	Linearity Analysis of Gate Engineered Dopingless and Junctionless Silicon Nanowire FET. , 2019, , .		2
32	Design and performance analysis of GAA Schottky barrier-gate stack-dopingless nanowire FET for phosphine gas detection. Applied Physics A: Materials Science and Processing, 2019, 125, 1.	2.3	16
33	Nanocantilever tri-gate junctionless cuboidal nanowire-FET-based directional pressure sensor. Applied Physics A: Materials Science and Processing, 2019, 125, 1.	2.3	8
34	Performance Assessment of the Charge-Plasma-Based Cylindrical GAA Vertical Nanowire TFET With Impact of Interface Trap Charges. IEEE Transactions on Electron Devices, 2019, 66, 4453-4460.	3.0	66
35	Design and Investigation of Charge-Plasma-Based Work Function Engineered Dual-Metal-Heterogeneous Gate Si-Si_{0.55}Ge_{0.45} GAA-Cylindrical NWTFET for Ambipolar Analysis. IEEE Transactions on Electron Devices, 2019, 66, 1468-1474.	3.0	44
36	Low Power and High Frequency Voltage Controlled Oscillator for PLL Application. , 2019, , .		4

#	Article	IF	Citations
37	Design and analysis of electrostatic-charge plasma based dopingless IGZO vertical nanowire FET for ammonia gas sensing. Superlattices and Microstructures, 2019, 125, 256-270.	3.1	28
38	Design and Analysis of Source Engineered with High Electron Mobility Material Triple Gate Junctionless Field Effect Transistor. Journal of Nanoelectronics and Optoelectronics, 2019, 14, 825-832.	0.5	2
39	A dopingless gate-all-around (GAA) gate-stacked nanowire FET with reduced parametric fluctuation effects. Journal of Computational Electronics, 2018, 17, 967-976.	2.5	19
40	Gate-All-Around Charge Plasma-Based Dual Material Gate-Stack Nanowire FET for Enhanced Analog Performance. IEEE Transactions on Electron Devices, 2018, 65, 3026-3032.	3.0	51
41	Multiband Microstrip Patch Antenna Design for 5G Using Metamaterial Structure. , 2018, , .		7
42	Design and Analysis of Pressure Sensor Based on MEMS Cantilever Structure and Pocket Doped DG-TFET. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 1295-1304.	0.5	6
43	A novel high mobility In1-xGaxAs cylindrical-gate-nanowire FET for gas sensing application with enhanced sensitivity. Superlattices and Microstructures, 2017, 111, 518-528.	3.1	35
44	Design and optimization analysis of dual material gate on DG-IMOS. Journal of Semiconductors, 2017, 38, 124003.	3.7	7
45	Pressure sensor based on MEMS nano-cantilever beam structure as a heterodielectric gate electrode of dopinglessÂTFET. Superlattices and Microstructures, 2016, 100, 535-547.	3.1	11
46	Design and analysis of RF-low power and low-phase noise CMOS ring oscillator for fully integrated RF communication systems technologies. International Journal of Information and Communication Technology, 2016, 8, 79.	0.1	0
47	Notice of Retraction Designing of Phase and Frequency Detector for low Jitter and high speed applications. , 2015, , .		1
48	The design of a novel delay cell based 8.3 GHz, low phase noise ring oscillator in C-MOS 180 nm technology for biomedical ultra-wide-band integrated applications. International Journal of Biomedical Engineering and Technology, 2013, 13, 1.	0.2	1
49	Design and Investigative Aspects of RF-Low Power 0.18-Âµm based CMOS Differential Ring Oscillator. International Journal of Advanced Science and Technology, 2013, 58, 87-102.	0.3	1
50	Low power ALU design by ancient mathematics. , 2010, , .		19
51	Small area reconfigurable FFT design by Vedic Mathematics. , 2010, , .		8
52	Performance Enhancement and Signal Distortion Analysis of Virtually Doped Nanotube Tunnel FET with Embedded Ferroelectric Gate Oxide. Silicon, 0, , 1.	3.3	1
53	Junctionless Silicon Nanotube Tunnel Field Effect Transistor Based Resistive Temperature Detector. Silicon, 0, , 1.	3.3	3
54	Design Considerations and Optimization of Electrostatic Doped Ferroelectric Nanotube Tunnel FET: Analog and Noise Analysis. Silicon, 0, , 1.	3.3	4