Hoi-Jun Yoo

List of Publications by Year in Descending Order

173 papers	2,726 citations	25 h-index	46 g-index
236 ext. papers	3,609 ext. citations	4.6 avg, IF	5.61 L-index

#	Paper	IF	Citations
173	OmniDRL: An Energy-Efficient Deep Reinforcement Learning Processor With Dual-Mode Weight Compression and Sparse Weight Transposer. *IEEE Journal of Solid-State Circuits*, **2022**, 1-1	5.5	
172	TSUNAMI: Triple Sparsity-Aware Ultra Energy-Efficient Neural Network Training Accelerator With Multi-Modal Iterative Pruning. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2022**, 1-13	3.9	
171	A Low-Power Graph Convolutional Network Processor With Sparse Grouping for 3D Point Cloud Semantic Segmentation in Mobile Devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2022**, 1-12	3.9	0
170	A 49.5 mW Multi-scale Linear Quantized Online Learning Processor for Real-Time Adaptive Object Detection. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	1
169	A 36.2 dB High SNR and PVT/Leakage-robust eDRAM Computing-In-Memory Macro with Segmented BL and Reference Cell Array. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	0
168	A Mobile DNN Training Processor with Automatic Bit-precision Search and Fine-grained Sparsity Exploitation. *IEEE Micro*, **2021**, 1-1	1.8	
167	An Overview of Sparsity Exploitation in CNNs for On-Device Intelligence With Software-Hardware Cross-Layer Optimizations. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2021**, 11, 634-648	5.2	2
166	An Overview of Energy-Efficient Hardware Accelerators for On-Device Deep-Neural-Network Training. *IEEE Open Journal of the Solid-State Circuits Society*, **2021**, 1, 115-128		3
165	. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1700-1704	3.5	0
164	DF-LNPU: A Pipelined Direct Feedback Alignment-Based Deep Neural Network Learning Processor for Fast Online Learning. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 1630-1640	5.5	2
163	A 64.1mW Accurate Real-Time Visual Object Tracking Processor With Spatial Early Stopping on Siamese Network. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1675-1679	3.5	4
162	A 43.1TOPS/W Energy-Efficient Absolute-Difference-Accumulation Operation Computing-In-Memory With Computation Reuse. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1605-1609	3.5	0
161	A 36-Channel Auto-Calibrated Front-End ASIC for a pMUT-Based Miniaturized 3-D Ultrasound System. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 1910-1923	5.5	6
160	. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 887-898	5.5	5
159	ECIM: Exponent Computing in Memory for an Energy Efficient Heterogeneous Floating-Point DNN Training Processor. *IEEE Micro*, **2021**, 1-1	1.8	2
158	A Pipelined Point Cloud Based Neural Network Processor for 3-D Vision With Large-Scale Max Pooling Layer Prediction. *IEEE Journal of Solid-State Circuits*, **2021**, 1-1	5.5	1
157	. *IEEE Solid-State Circuits Letters*, **2021**, 4, 22-25	2	2

156	GANPU: An Energy-Efficient Multi-DNN Training Processor for GANs With Speculative Dual-Sparsity Exploitation. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 2845-2857	5.5	5
155	HNPU: An Adaptive DNN Training Processor Utilizing Stochastic Dynamic Fixed-Point and Active Bit-Precision Searching. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 2858-2869	5.5	10
154	An Energy-Efficient GAN Accelerator With On-Chip Training for Domain-Specific Optimization. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 2968-2980	5.5	2
153	Simultaneous Electrical Bio-Impedance Plethysmography at Different Body Parts: Continuous and Non-Invasive Monitoring of Pulse Wave Velocity. *IEEE Transactions on Biomedical Circuits and Systems*, **2021**, 15, 1027-1038	5.1	3
152	Design of Sub-10-μW Sub-0.1% THD Sinusoidal Current Generator IC for Bio-Impedance Sensing. *IEEE Journal of Solid-State Circuits*, **2021**, 1-1	5.5	1
151	DT-CNN: An Energy-Efficient Dilated and Transposed Convolutional Neural Network Processor for Region of Interest Based Image Segmentation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 3471-3483	3.9	7
150	The Development of Silicon for AI: Different Design Approaches. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 4719-4732	3.9	4
149	A 0.5-V Sub-10-μW 15.28-mΩ@1Hz Bio-Impedance Sensor IC With Sub-1° Phase Error. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2161-2173	5.5	8
148	A 9.6 mW/Ch 10 MHz Wide-bandwidth Electrical Impedance Tomography IC with Accurate Phase Compensation for Breast Cancer Detection **2020**,		5
147	A 1.15 TOPS/W Energy-Efficient Capsule Network Accelerator for Real-Time 3D Point Cloud Segmentation in Mobile Environment. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1594-1598	3.5	3
146	A Power-Efficient CNN Accelerator With Similar Feature Skipping for Face Recognition in Mobile Devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 1181-1193	3.9	9
145	A 0.22–0.89 mW Low-Power and Highly-Secure Always-On Face Recognition Processor With Adversarial Attack Prevention. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 846-850	3.5	3
144	7.4 GANPU: A 135TFLOPS/W Multi-DNN Training Processor for GANs with Speculative Dual-Sparsity Exploitation **2020**,		24
143	Neuro-inspired computing chips. *Nature Electronics*, **2020**, 3, 371-382	28.4	139
142	SRNPU: An Energy-Efficient CNN-Based Super-Resolution Processor With Tile-Based Selective Super-Resolution in Mobile Devices. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2020**, 10, 320-334	5.2	9
141	Wireless Body-Area-Network Transceiver and Low-Power Receiver With High Application Expandability. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2781-2789	5.5	6
140	Z-PIM: An Energy-Efficient Sparsity Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision **2020**,		10
139	A 146.52 TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping **2020**,		8

138	A 4.45 ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices **2020**,		2
137	A 54.7 fps 3D Point Cloud Semantic Segmentation Processor with Sparse Grouping Based Dilated Graph Convolutional Network for Mobile Devices **2020**,		1
136	A 1.02-W STT-MRAM-Based DNN ECG Arrhythmia Monitoring SoC With Leakage-Based Delay MAC Unit. *IEEE Solid-State Circuits Letters*, **2020**, 3, 390-393	2	6
135	The Hardware and Algorithm Co-Design for Energy-Efficient DNN Processor on Edge/Mobile Devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 3458-3470	3.9	13
134	. *Proceedings of the IEEE*, **2020**, 108, 1245-1260	14.3	11
133	An Energy-Efficient Deep Reinforcement Learning Accelerator With Transposable PE Array and Experience Compression. *IEEE Solid-State Circuits Letters*, **2019**, 2, 228-231	2	4
132	DT-CNN: Dilated and Transposed Convolution Neural Network Accelerator for Real-Time Image Segmentation on Mobile Devices **2019**,		12
131	A 15.2 TOPS/W CNN Accelerator with Similar Feature Skipping for Face Recognition in Mobile Devices **2019**,		3
130	**2019**,		59
129	A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression **2019**,		17
128	Understanding Body Channel Communication : A review: from history to the future applications **2019**,		1
127	CNNP-v2:An Energy Efficient Memory-Centric Convolutional Neural Network Processor Architecture **2019**,		4
126	A 1.32 TOPS/W Energy Efficient Deep Neural Network Learning Processor with Direct Feedback Alignment based Heterogeneous Core Architecture **2019**,		14
125	Custom Sub-Systems and Circuits for Deep Learning: Guest Editorial Overview. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2019**, 9, 247-252	5.2	2
124	Direct Feedback Alignment Based Convolutional Neural Network Training for Low-Power Online Learning Processor **2019**,		2
123	An 802.15.6 HBC Standard Compatible Transceiver and 90 pJ/b Full-Duplex Transceiver for Body Channel Communication **2019**,		2
122	CNNP-v2: A Memory-Centric Architecture for Low-Power CNN Processor on Domain-Specific Mobile Devices. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2019**, 9, 598-611	5.2	3
121	. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 1185-1195	5.5	14

120	A Low-Power Deep Neural Network Online Learning Processor for Real-Time Object Tracking Application. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 1794-1804	3.9	22
119	UNPU: An Energy-Efficient Deep Neural Network Accelerator With Fully Variable Weight Bit Precision. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 173-185	5.5	103
118	A Low-Power Convolutional Neural Network Face Recognition Processor and a CIS Integrated With Always-on Face Detector. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 115-123	5.5	39
117	4-Camera VGA-resolution capsule endoscope with 80Mb/s body-channel communication transceiver and Sub-cm range capsule localization **2018**,		13
116	An EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 1830-1843	5.5	32
115	UNPU: A 50.6TOPS/W unified deep neural network accelerator with 1b-to-16b fully-variable weight bit-precision **2018**,		151
114	**2018**,		20
113	A 46.1 fps Global Matching Optical Flow Estimation Processor for Action Recognition in Mobile Devices **2018**,		1
112	Toward all-day wearable health monitoring: An ultralow-power, reflective organic pulse oximetry sensing patch. *Science Advances*, **2018**, 4, eaas9530	14.3	93
111	DNPU: An Energy-Efficient Deep-Learning Processor with Heterogeneous Multi-Core Architecture. *IEEE Micro*, **2018**, 38, 85-93	1.8	24
110	A 141.4 mW Low-Power Online Deep Neural Network Training Processor for Real-time Object Tracking in Mobile Devices **2018**,		7
109	A 17.5-fJ/bit Energy-Efficient Analog SRAM for Mixed-Signal Processing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2714-2723	2.6	9
108	14.2 DNPU: An 8.1TOPS/W reconfigurable CNN-RNN processor for general-purpose deep neural networks **2017**,		157
107	A 82-nW Chaotic Map True Random Number Generator Based on a Sub-Ranging SAR ADC. *IEEE Journal of Solid-State Circuits*, **2017**, 52, 1953-1965	5.5	37
106	An energy-efficient deep learning processor with heterogeneous multi-core architecture for convolutional neural networks and recurrent neural networks **2017**,		3
105	A 0.53mW ultra-low-power 3D face frontalization processor for face recognition with human-level accuracy in wearable devices **2017**,		1
104	A 31.2pJ/disparity□pixel stereo matching processor with stereo SRAM for mobile UI application **2017**,		2
103	. *IEEE Journal of Solid-State Circuits*, **2017**, 52, 139-150	5.5	16

102	An ultra-low-power and mixed-mode event-driven face detection SoC for always-on mobile applications **2017**,		9
101	A 1.4-m $Omega$ -Sensitivity 94-dB Dynamic-Range Electrical Impedance Tomography SoC and 48-Channel Hub-SoC for 3-D Lung Ventilation Monitoring System. *IEEE Journal of Solid-State Circuits*, **2017**, 52, 2829-2842	5.5	24
100	A multimodal headpatch system for patient brain monitoring in OR and PACU **2017**,		1
99	A 21mW low-power recurrent neural network accelerator with quantization tables for embedded deep learning applications **2017**,		10
98	A 1GHz fault tolerant processor with dynamic lockstep and self-recovering cache for ADAS SoC complying with ISO26262 in automotive electronics **2017**,		6
97	A 590MDE/s semi-global matching processor with lossless data compression **2017**,		1
96	A CMOS Image Sensor-Based Stereo Matching Accelerator With Focal-Plane Sparse Rectification and Analog Census Transform. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 2180-2188	3.9	3
95	A 540-[Formula: see text] Duty Controlled RSSI With Current Reusing Technique for Human Body Communication. *IEEE Transactions on Biomedical Circuits and Systems*, **2016**, 10, 893-901	5.1	2
94	A Fault-Tolerant Cache System of Automotive Vision Processor Complying With ISO26262. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 1146-1150	3.5	3
93	A 82nW chaotic-map true random number generator based on sub-ranging SAR ADC **2016**,		9
92	A fabric wrist patch sensor for continuous and comprehensive monitoring of the cardiovascular system. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2016**, 2016, 6070-6073	0.9	3
91	A 0.5 V 54 $mutext{W}$ Ultra-Low-Power Object Matching Processor for Micro Air Vehicle Navigation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 359-369	3.9	4
90	14.1 A 126.1mW real-time natural UI/UX processor with embedded deep-learning core for low-power smart glasses **2016**,		17
89	A 2.71 nJ/Pixel Gaze-Activated Object Recognition System for Low-Power Mobile Smart Glasses. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 45-55	5.5	11
88	A 43.7 mW 94 fps CMOS image sensor-based stereo matching accelerator with focal-plane rectification and analog census transformation **2016**,		2
87	Circuits and Systems for Wireless Body Area Network **2016**, 375-403		
86	A 635 □W non-contact compensation IC for body channel communication **2016**,		2
85	A multimodal drowsiness monitoring ear-module system with closed-loop real-time alarm **2016**,		6

84	A 0.5Error 10 mW CMOS Image Sensor-Based Gaze Estimation Processor. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 1032-1040	5.5	3
83	30-fps SNR equalized electrical impedance tomography IC with fast-settle filter and adaptive current control for lung monitoring **2016**,		2
82	An Energy-Efficient Embedded Deep Neural Network Processor for High Speed Visual Attention in Mobile Vision Recognition SoC. *IEEE Journal of Solid-State Circuits*, **2016**, 1-9	5.5	9
81	The Effects of Electrode Configuration on Body Channel Communication Based on Analysis of Vertical and Horizontal Electric Dipoles. *IEEE Transactions on Microwave Theory and Techniques*, **2015**, 63, 1409-1420	4.1	31
80	A 45 muW Injection-Locked FSK Wake-Up Receiver With Frequency-to-Envelope Conversion for Crystal-Less Wireless Body Area Network. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 1351-1360	5.5	27
79	4.6 A1.93TOPS/W scalable deep learning/inference processor with tetra-parallel MIMD architecture for big-data applications **2015**,		41
78	K-glass: Real-time markerless augmented reality smart glasses platform **2015**,		1
77	A 0.54-mW duty controlled RSSI with current reusing technique for human body communication **2015**,		2
76	. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 2549-2559	5.5	25
75	A keypoint-level parallel pipelined object recognition processor with gaze activation image sensor for mobile smart glasses system **2015**,		1
74	A 27 mW Reconfigurable Marker-Less Logarithmic Camera Pose Estimation Engine for Mobile Augmented Reality Processor. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 2513-2523	5.5	8
73	A 10.4 mW Electrical Impedance Tomography SoC for Portable Real-Time Lung Ventilation Monitoring System. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 2501-2512	5.5	29
72	A 1.22 TOPS and 1.52 mW/MHz Augmented Reality Multicore Processor With Neural Network NoC for HMD Applications. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 113-124	5.5	13
71	. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 245-257	5.5	69
70	A Vocabulary Forest Object Matching Processor With 2.07 M-Vector/s Throughput and 13.3 nJ/Vector Per-Vector Energy for Full-HD 60 fps Video Object Recognition. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 1059-1069	5.5	10
69	Intelligent task scheduler with high throughput NoC for real-time mobile object recognition SoC **2015**,		2
68	79pJ/b 80Mb/s full-duplex transceiver and 42.5jiW 100kb/s super-regenerative transceiver for body channel communication **2015**,		1
67	An Impedance and Multi-Wavelength Near-Infrared Spectroscopy IC for Non-Invasive Blood Glucose Estimation. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 1025-1037	5.5	50

66	A 1.5nJ/pixel super-resolution enhanced FAST corner detection processor for high accuracy AR **2014**,		1
65	An 87-$hbox{mA}cdot min$ Iontophoresis Controller IC With Dual-Mode Impedance Sensor for Patch-Type Transdermal Drug Delivery System. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 167-178	5.5	11
64	A 33W/node Duty Cycle Controlled HBC Transceiver system for medical BAN with 64 sensor nodes **2014**,		3
63	An 1.61mW mixed-signal column processor for BRISK feature extraction in CMOS image sensor **2014**,		3
62	3.8 mW electrocardiogram (ECG) filtered electrical impedance tomography IC using I/Q homodyne architecture for breast cancer diagnosis **2014**,		2
61	Energy-efficient Mixed-mode support vector machine processor with analog Gaussian kernel **2014**,		1
60	A 4.9 mW neural network task scheduler for congestion-minimized network-on-chip in multi-core systems **2014**,		4
59	Intelligent Network-on-Chip With Online Reinforcement Learning for Portable HD Object Recognition Processor. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 476-484	3.9	6
58	1.2-mW Online Learning Mixed-Mode Intelligent Inference Engine for Low-Power Real-Time Object Recognition Processor. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 921-933	2.6	11
57	A 320 mW 342 GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 33-45	5.5	23
56	A 37.5 /spl mu/W Body Channel Communication Wake-Up Receiver With Injection-Locking Ring Oscillator for Wireless Body Area Network. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2013**, 60, 1200-1208	3.9	26
55	A 57 mW 12.5 μJ/Epoch Embedded Mixed-Mode Neuro-Fuzzy Processor for Mobile Real-Time Object Recognition. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 2894-2907	5.5	9
54	A high-throughput 16super resolution processor for real-time object recognition SoC **2013**,		1
53	. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 2678-2692	5.5	39
52	An energy-efficient body channel communication based on Maxwell's equations analysis of on-body transmission mechanism **2012**,		7
51	A 46 W motion artifact reduction bio-signal sensor with ICA based adaptive DC level control for sleep monitoring system **2012**,		2
50	Online Reinforcement Learning NoC for portable HD object recognition processor **2012**,		1
49	A 92-mW Real-Time Traffic Sign Recognition System With Robust Illumination Adaptation and Support Vector Machine. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 2711-2723	5.5	10

48	. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 353-364	5.5	89
47	. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 42-51	5.5	39
46	A 57mW embedded mixed-mode neuro-fuzzy accelerator for intelligent multi-core processor **2011**,		6
45	An asynchronous mixed-mode neuro-fuzzy controller for energy efficient machine intelligence SoC **2011**,		1
44	A 92mW real-time traffic sign recognition system with robust light and dark adaptation **2011**,		4
43	A 20 μW contact impedance sensor for wireless body-area-network transceiver **2011**,		5
42	24-GOPS 4.5- mm digital cellular neural network for rapid visual attention in an object-recognition SoC. *IEEE Transactions on Neural Networks*, **2011**, 22, 64-73		25
41	A low energy crystal-less double-FSK transceiver for wireless body-area-network **2011**,		5
40	A 145 W 8 parallel multiplier based on optimized bypassing architecture **2011**,		1
39	A 30fps stereo matching processor based on belief propagation with disparity-parallel PE array architecture **2010**,		9
38	A wirelessly-powered electro-acupuncture based on Adaptive Pulse Width Mono-Phase stimulation **2010**,		1
37	Live demonstration: A real-time compensated inductive transceiver for wearable MP3 player system on multi-layered planar fashionable circuit board **2010**,		1
36	Wireless fabric patch sensors for wearable healthcare. *Annual International Conference of the IEEE Engineering in Medicine and Biology Society IEEE Engineering in Medicine and Biology Society Annual International Conference*, **2010**, 2010, 5254-7	0.9	3
35	Intelligent NoC with neuro-fuzzy bandwidth regulation for a 51 IP object recognition processor **2010**,		4
34	Electrical Characterization of Screen-Printed Circuits on the Fabric. *IEEE Transactions on Advanced Packaging*, **2010**, 33, 196-205		101
33	. *IEEE Journal of Solid-State Circuits*, **2010**, 45, 32-45	5.5	82
32	A 0.5-mu V$_{rm rms}$ 12-mu W Wirelessly Powered Patch-Type Healthcare Sensor for Wearable Body Sensor Network. *IEEE Journal of Solid-State Circuits*, **2010**,	5.5	7
31	A Low-Energy Inductive Coupling Transceiver With Cm-Range 50-Mbps Data Communication in Mobile Device Applications. *IEEE Journal of Solid-State Circuits*, **2010**,	5.5	11

30	A 92m W 76.8GOPS vector matching processor with parallel Huffman decoder and query re-ordering buffer for real-time object recognition **2010**,		3
29	A low power ECG signal processor for ambulatory arrhythmia monitoring system **2010**,		23
28	A 200-Mbps 0.02-nJ/b Dual-Mode Inductive Coupling Transceiver for cm-Range Multimedia Application. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2009**, 56, 1063-1072	3.9	15
27	A Planar MICS Band Antenna Combined With a Body Channel Communication Electrode for Body Sensor Network. *IEEE Transactions on Microwave Theory and Techniques*, **2009**, 57, 2515-2522	4.1	39
26	A Wearable Fabric Computer by Planar-Fashionable Circuit Board Technique **2009**,		23
25	A 152-mW Mobile Multimedia SoC With Fully Programmable 3-D Graphics and MPEG4/H.264/JPEG. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 1260-1266	2.6	4
24	. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 136-147	5.5	33
23	Power and Area-Efficient Unified Computation of Vector and Elementary Functions for Handheld 3D Graphics Systems. *IEEE Transactions on Computers*, **2008**, 57, 490-504	2.5	54
22	A 195 mW, 9.1 MVertices/s Fully Programmable 3-D Graphics Processor for Low-Power Mobile Devices. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 2370-2380	5.5	6
21	A 76.8 GB/s 46 mW low-latency network-on-chip for real-time object recognition processor **2008**,		3
20	The brain mimicking Visual Attention Engine: An 80□0 digital Cellular Neural Network for rapid global feature extraction **2008**,		3
19	A low energy bio sensor node processor for continuous healthcare monitoring system **2008**,		6
18	A Low Power 16-bit RISC with Lossless Compression Accelerator for Body Sensor Network System **2006**,		9
17	A 231MHz, 2.18mW 32-bit Logarithmic Arithmetic Unit for Fixed-Point 3D Graphics System **2005**,		4
16	Networks-on-chip and Networks-in-Package for High-Performance SoC Platforms **2005**,		7
15	Packet-switched on-chip interconnection network for system-on-chip applications. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2005**, 52, 308-312		20
14	1.25-Gb/s regulated cascode CMOS transimpedance amplifier for Gigabit Ethernet applications. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 112-121	5.5	199
13	1-Gb/s 80-dB/spl Omega/ fully differential CMOS transimpedance amplifier in multichip on oxide technology for optical interconnects. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 971-974	5.5	24

12	Race logic architecture (RALA): a novel logic concept using the race scheme of input variables. *IEEE Journal of Solid-State Circuits*, **2002**, 37, 191-201	5.5	5
11	A 120-mW 3-D rendering engine with 6-Mb embedded DRAM and 3.2-GB/s runtime reconfigurable bus for PDA chip. *IEEE Journal of Solid-State Circuits*, **2002**, 37, 1352-1355	5.5	5
10	A reconfigurable multilevel parallel texture cache memory with 75-GB/s parallel cache replacement bandwidth. *IEEE Journal of Solid-State Circuits*, **2002**, 37, 612-623	5.5	3
9	A 7.1-GB/s low-power rendering engine in 2-D array-embedded memory logic CMOS for portable multimedia system. *IEEE Journal of Solid-State Circuits*, **2001**, 36, 944-955	5.5	16
8	Dual-V/sub T/ self-timed CMOS logic for low subthreshold current multigigabit synchronous DRAM. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **1998**, 45, 1263-1271		7
7	A low-noise folded bit-line sensing architecture for multigigabit DRAM with ultrahigh-density 6F/sup 2/ cell [CMOS design]. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 1096-1102	5.5	2
6	Diffusion of zinc into gaas through Al0.3Ga00.7As. *Journal of Electronic Materials*, **1988**, 17, 337-339	1.9	2
5	A small ripple regulated charge pump with automatic pumping control schemes		6
4	An arbitration look-ahead scheme for reducing end-to-end latency in networks on chip		3
3	Optimization of portable system architecture for real-time 3D graphics		3
2	A 670 ps, 64 bit dynamic low-power adder design		4
1	Design and implementation of CMOS LVDS 2.5 Gb/s transmitter and 1.3 Gb/s receiver for optical interconnections		8