

Hoi-Jun Yoo

List of Publications by Year in descending order

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236
all docs

236
docs citations

236
times ranked

3767
citing authors

#	ARTICLE	IF	CITATIONS
1	Neuro-inspired computing chips. Nature Electronics, 2020, 3, 371-382.	26.0	402
2	1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications. IEEE Journal of Solid-State Circuits, 2004, 39, 112-121.	5.4	270
3	14.2 DNPU: An 8.1TOPS/W reconfigurable CNN-RNN processor for general-purpose deep neural networks. , 2017, , .		228
4	UNPU: A 50.6TOPS/W unified deep neural network accelerator with 1b-to-16b fully-variable weight bit-precision. , 2018, , .		226
5	UNPU: An Energy-Efficient Deep Neural Network Accelerator With Fully Variable Weight Bit Precision. IEEE Journal of Solid-State Circuits, 2019, 54, 173-185.	5.4	199
6	Toward all-day wearable health monitoring: An ultralow-power, reflective organic pulse oximetry sensing patch. Science Advances, 2018, 4, eaas9530.	10.3	171
7	Electrical Characterization of Screen-Printed Circuits on the Fabric. IEEE Transactions on Advanced Packaging, 2010, 33, 196-205.	1.6	134
8	7.7 LNPU: A 25.3TFLOPS/W Sparse Deep-Neural-Network Learning Processor with Fine-Grained Mixed Precision of FP8-FP16. , 2019, , .		111
9	A 3.9 mW 25-Electrode Reconfigured Sensor for Wearable Cardiac Monitoring System. IEEE Journal of Solid-State Circuits, 2011, 46, 353-364.	5.4	107
10	A 4.9 mΩ-Sensitivity Mobile Electrical Impedance Tomography IC for Early Breast-Cancer Detection System. IEEE Journal of Solid-State Circuits, 2015, 50, 245-257.	5.4	107
11	A 201.4 GOPS 496 mW Real-Time Multi-Object Recognition Processor With Bio-Inspired Neural Perception Engine. IEEE Journal of Solid-State Circuits, 2010, 45, 32-45.	5.4	100
12	A Low-Power Convolutional Neural Network Face Recognition Processor and a CIS Integrated With Always-on Face Detector. IEEE Journal of Solid-State Circuits, 2018, 53, 115-123.	5.4	76
13	An Impedance and Multi-Wavelength Near-Infrared Spectroscopy IC for Non-Invasive Blood Glucose Estimation. IEEE Journal of Solid-State Circuits, 2015, 50, 1025-1037.	5.4	75
14	A 82-nW Chaotic Map True Random Number Generator Based on a Sub-Ranging SAR ADC. IEEE Journal of Solid-State Circuits, 2017, 52, 1953-1965.	5.4	71
15	Power and Area-Efficient Unified Computation of Vector and Elementary Functions for Handheld 3D Graphics Systems. IEEE Transactions on Computers, 2008, 57, 490-504.	3.4	68
16	A 345 mW Heterogeneous Many-Core Processor With an Intelligent Inference Engine for Robust Object Recognition. IEEE Journal of Solid-State Circuits, 2011, 46, 42-51.	5.4	61
17	4.6 A1.93TOPS/W scalable deep learning/inference processor with tetra-parallel MIMD architecture for big-data applications. , 2015, , .		56
18	A Low-Energy Crystal-Less Double-FSK Sensor Node Transceiver for Wireless Body-Area Network. IEEE Journal of Solid-State Circuits, 2012, 47, 2678-2692.	5.4	54

#	ARTICLE	IF	CITATIONS
19	An EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring. IEEE Journal of Solid-State Circuits, 2018, 53, 1830-1843.	5.4	52
20	7.4 GANPU: A 135TFLOPS/W Multi-DNN Training Processor for GANs with Speculative Dual-Sparsity Exploitation. , 2020, , .		51
21	A 10.4 mW Electrical Impedance Tomography SoC for Portable Real-Time Lung Ventilation Monitoring System. IEEE Journal of Solid-State Circuits, 2015, 50, 2501-2512.	5.4	48
22	A Planar MICS Band Antenna Combined With a Body Channel Communication Electrode for Body Sensor Network. IEEE Transactions on Microwave Theory and Techniques, 2009, 57, 2515-2522.	4.6	46
23	A 37.5 μ W Body Channel Communication Wake-Up Receiver With Injection-Locking Ring Oscillator for Wireless Body Area Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1200-1208.	5.4	45
24	A 1.4-m Ω -Sensitivity 94-dB Dynamic-Range Electrical Impedance Tomography SoC and 48-Channel Hub-SoC for 3-D Lung Ventilation Monitoring System. IEEE Journal of Solid-State Circuits, 2017, 52, 2829-2842.	5.4	44
25	DNPU: An Energy-Efficient Deep-Learning Processor with Heterogeneous Multi-Core Architecture. IEEE Micro, 2018, 38, 85-93.	1.8	44
26	A 125 GOPS 583 mW Network-on-Chip Based Parallel Processor With Bio-Inspired Visual Attention Engine. IEEE Journal of Solid-State Circuits, 2009, 44, 136-147.	5.4	43
27	A 45 μ W Injection-Locked FSK Wake-Up Receiver With Frequency-to-Envelope Conversion for Crystal-Less Wireless Body Area Network. IEEE Journal of Solid-State Circuits, 2015, 50, 1351-1360.	5.4	40
28	A Low-Power Deep Neural Network Online Learning Processor for Real-Time Object Tracking Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1794-1804.	5.4	37
29	A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression. , 2019, , .		36
30	HNPU: An Adaptive DNN Training Processor Utilizing Stochastic Dynamic Fixed-Point and Active Bit-Precision Searching. IEEE Journal of Solid-State Circuits, 2021, 56, 2858-2869.	5.4	36
31	The Effects of Electrode Configuration on Body Channel Communication Based on Analysis of Vertical and Horizontal Electric Dipoles. IEEE Transactions on Microwave Theory and Techniques, 2015, 63, 1409-1420.	4.6	35
32	A 9.02mW CNN-stereo-based real-time 3D hand-gesture recognition processor for smart mobile devices. , 2018, , .		34
33	A 5.2 mW IEEE 802.15.6 HBC Standard Compatible Transceiver With Power Efficient Delay-Locked-Loop Based BPSK Demodulator. IEEE Journal of Solid-State Circuits, 2015, 50, 2549-2559.	5.4	33
34	1-Gb/s 80-dB/spl Ω / fully differential CMOS transimpedance amplifier in multichip on oxide technology for optical interconnects. IEEE Journal of Solid-State Circuits, 2004, 39, 971-974.	5.4	31
35	A Wearable Fabric Computer by Planar-Fashionable Circuit Board Technique. , 2009, , .		30
36	24-GOPS 4.5- μ m Digital Cellular Neural Network for Rapid Visual Attention in an Object-Recognition SoC. IEEE Transactions on Neural Networks, 2011, 22, 64-73.	4.2	30

#	ARTICLE	IF	CITATIONS
37	SRNPU: An Energy-Efficient CNN-Based Super-Resolution Processor With Tile-Based Selective Super-Resolution in Mobile Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 320-334.	3.6	29
38	A low power ECG signal processor for ambulatory arrhythmia monitoring system. , 2010, , .		28
39	A 1.32 TOPS/W Energy Efficient Deep Neural Network Learning Processor with Direct Feedback Alignment based Heterogeneous Core Architecture. , 2019, , .		28
40	4-Camera VGA-resolution capsule endoscope with 80Mb/s body-channel communication transceiver and Sub-cm range capsule localization. , 2018, , .		26
41	DT-CNN: Dilated and Transposed Convolution Neural Network Accelerator for Real-Time Image Segmentation on Mobile Devices. , 2019, , .		26
42	A 0.8-V 82.9- μ W In-Ear BCI Controller IC With 8.8 PEF EEG Instrumentation Amplifier and Wireless BAN Transceiver. IEEE Journal of Solid-State Circuits, 2019, 54, 1185-1195.	5.4	26
43	The Heterogeneous Deep Neural Network Processor With a Non-von Neumann Architecture. Proceedings of the IEEE, 2020, 108, 1245-1260.	21.3	26
44	A 36-Channel Auto-Calibrated Front-End ASIC for a pMUT-Based Miniaturized 3-D Ultrasound System. IEEE Journal of Solid-State Circuits, 2021, 56, 1910-1923.	5.4	26
45	Packet-switched on-chip interconnection network for system-on-chip applications. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 308-312.	2.2	25
46	A 502-GOPS and 0.984-mW Dual-Mode Intelligent ADAS SoC With Real-Time Semiglobal Matching and Intention Prediction for Smart Automotive Black Box System. IEEE Journal of Solid-State Circuits, 2017, 52, 139-150.	5.4	25
47	The Hardware and Algorithm Co-Design for Energy-Efficient DNN Processor on Edge/Mobile Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3458-3470.	5.4	25
48	A 1.22 TOPS and 1.52 mW/MHz Augmented Reality Multicore Processor With Neural Network NoC for HMD Applications. IEEE Journal of Solid-State Circuits, 2015, 50, 113-124.	5.4	24
49	DT-CNN: An Energy-Efficient Dilated and Transposed Convolutional Neural Network Processor for Region of Interest Based Image Segmentation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3471-3483.	5.4	24
50	A 320 mW 342 GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams. IEEE Journal of Solid-State Circuits, 2013, 48, 33-45.	5.4	23
51	14.1 A 126.1mW real-time natural UI/UX processor with embedded deep-learning core for low-power smart glasses. , 2016, , .		22
52	A 0.5- μ V $_{\text{rms}}$ 12- μ W Wirelessly Powered Patch-Type Healthcare Sensor for Wearable Body Sensor Network. IEEE Journal of Solid-State Circuits, 2010, , .	5.4	21
53	A 146.52 TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping. , 2020, , .		21
54	A 0.5-V Sub-10- $\frac{1}{4}$ W 15.28-m $\frac{1}{\text{s}}$ Hz Bio-Impedance Sensor IC With Sub-1 $^{\circ}$ Phase Error. IEEE Journal of Solid-State Circuits, 2020, 55, 2161-2173.	5.4	20

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55	A Power-Efficient CNN Accelerator With Similar Feature Skipping for Face Recognition in Mobile Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1181-1193.	5.4	20
56	A 9.6-mW/Ch 10-MHz Wide-Bandwidth Electrical Impedance Tomography IC With Accurate Phase Compensation for Early Breast Cancer Detection. IEEE Journal of Solid-State Circuits, 2021, 56, 887-898.	5.4	20
57	A 200-Mbps 0.02-nJ/b Dual-Mode Inductive Coupling Transceiver for cm-Range Multimedia Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1063-1072.	5.4	19
58	An ultra-low-power and mixed-mode event-driven face detection SoC for always-on mobile applications. , 2017, , .		19
59	A Low-Energy Inductive Coupling Transceiver With Cm-Range 50-Mbps Data Communication in Mobile Device Applications. IEEE Journal of Solid-State Circuits, 2010, , .	5.4	18
60	An 87- μA \cdot min μW Iontophoresis Controller IC With Dual-Mode Impedance Sensor for Patch-Type Transdermal Drug Delivery System. IEEE Journal of Solid-State Circuits, 2014, 49, 167-178.	5.4	18
61	GANPU: An Energy-Efficient Multi-DNN Training Processor for GANs With Speculative Dual-Sparsity Exploitation. IEEE Journal of Solid-State Circuits, 2021, 56, 2845-2857.	5.4	18
62	A 7.1-GB/s low-power rendering engine in 2-D array-embedded memory logic CMOS for portable multimedia system. IEEE Journal of Solid-State Circuits, 2001, 36, 944-955.	5.4	17
63	Z-PIM: An Energy-Efficient Sparsity Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision. , 2020, , .		17
64	A 2.71 nJ/Pixel Gaze-Activated Object Recognition System for Low-Power Mobile Smart Glasses. IEEE Journal of Solid-State Circuits, 2016, 51, 45-55.	5.4	15
65	A 17.5-fJ/bit Energy-Efficient Analog SRAM for Mixed-Signal Processing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2714-2723.	3.1	15
66	Wireless Body-Area-Network Transceiver and Low-Power Receiver With High Application Expandability. IEEE Journal of Solid-State Circuits, 2020, 55, 2781-2789.	5.4	15
67	DF-LNPU: A Pipelined Direct Feedback Alignment-Based Deep Neural Network Learning Processor for Fast Online Learning. IEEE Journal of Solid-State Circuits, 2021, 56, 1630-1640.	5.4	15
68	Design and implementation of CMOS LVDS 2.5 Gb/s transmitter and 1.3 Gb/s receiver for optical interconnections. , 0, , .		14
69	A Vocabulary Forest Object Matching Processor With 2.07 M-Vector/s Throughput and 13.3 nJ/Vector Per-Vector Energy for Full-HD 60 fps Video Object Recognition. IEEE Journal of Solid-State Circuits, 2015, 50, 1059-1069.	5.4	14
70	An Energy-Efficient Embedded Deep Neural Network Processor for High Speed Visual Attention in Mobile Vision Recognition SoC. IEEE Journal of Solid-State Circuits, 2016, , 1-9.	5.4	14
71	Simultaneous Electrical Bio-Impedance Plethysmography at Different Body Parts: Continuous and Non-Invasive Monitoring of Pulse Wave Velocity. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 1027-1038.	4.0	14
72	A 57 mW 12.5 μJ /Epoch Embedded Mixed-Mode Neuro-Fuzzy Processor for Mobile Real-Time Object Recognition. IEEE Journal of Solid-State Circuits, 2013, 48, 2894-2907.	5.4	13

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73	A 82nW chaotic-map true random number generator based on sub-ranging SAR ADC. , 2016, , .		13
74	A 21mW low-power recurrent neural network accelerator with quantization tables for embedded deep learning applications. , 2017, , .		13
75	A 1.02- μ W STT-MRAM-Based DNN ECG Arrhythmia Monitoring SoC With Leakage-Based Delay MAC Unit. IEEE Solid-State Circuits Letters, 2020, 3, 390-393.	2.0	13
76	Design of Sub-10- μ W Sub-0.1% THD Sinusoidal Current Generator IC for Bio-Impedance Sensing. IEEE Journal of Solid-State Circuits, 2022, 57, 586-595.	5.4	13
77	1.2-mW Online Learning Mixed-Mode Intelligent Inference Engine for Low-Power Real-Time Object Recognition Processor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 921-933.	3.1	12
78	A small ripple regulated charge pump with automatic pumping control schemes. , 0, , .		11
79	A Low Power 16-bit RISC with Lossless Compression Accelerator for Body Sensor Network System. , 2006, , .		11
80	A 92-mW Real-Time Traffic Sign Recognition System With Robust Illumination Adaptation and Support Vector Machine. IEEE Journal of Solid-State Circuits, 2012, 47, 2711-2723.	5.4	11
81	Intelligent Network-on-Chip With Online Reinforcement Learning for Portable HD Object Recognition Processor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 476-484.	5.4	11
82	A 27 mW Reconfigurable Marker-Less Logarithmic Camera Pose Estimation Engine for Mobile Augmented Reality Processor. IEEE Journal of Solid-State Circuits, 2015, 50, 2513-2523.	5.4	11
83	A 141.4 mW Low-Power Online Deep Neural Network Training Processor for Real-time Object Tracking in Mobile Devices. , 2018, , .		11
84	An Overview of Sparsity Exploitation in CNNs for On-Device Intelligence With Software-Hardware Cross-Layer Optimizations. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 634-648.	3.6	11
85	An Overview of Energy-Efficient Hardware Accelerators for On-Device Deep-Neural-Network Training. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 115-128.	2.7	11
86	Dual-V _T /self-timed CMOS logic for low subthreshold current multigigabit synchronous DRAM. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 1263-1271.	2.2	10
87	A 195 mW, 9.1 MVertices/s Fully Programmable 3-D Graphics Processor for Low-Power Mobile Devices. IEEE Journal of Solid-State Circuits, 2008, 43, 2370-2380.	5.4	10
88	An energy-efficient dual sampling SAR ADC with reduced capacitive DAC. , 2009, , .		10
89	A 30fps stereo matching processor based on belief propagation with disparity-parallel PE array architecture. , 2010, , .		10
90	Wireless fabric patch sensors for wearable healthcare. , 2010, 2010, 5254-7.		10

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91	A 57mW embedded mixed-mode neuro-fuzzy accelerator for intelligent multi-core processor. , 2011, , .		10
92	A 0.5 V 54 Ultra-Low-Power Object Matching Processor for Micro Air Vehicle Navigation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 359-369.	5.4	10
93	93.8% Current Efficiency and 0.672 ns Transient Response Reconfigurable LDO for Wireless Sensor Network Systems. , 2019, , .		10
94	The Development of Silicon for AI: Different Design Approaches. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4719-4732.	5.4	10
95	A 0.22â€“0.89 mW Low-Power and Highly-Secure Always-On Face Recognition Processor With Adversarial Attack Prevention. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 846-850.	3.0	10
96	PNPU: An Energy-Efficient Deep-Neural-Network Learning Processor With Stochastic Coarseâ€“Fine Level Weight Pruning and Adaptive Input/Output/Weight Zero Skipping. IEEE Solid-State Circuits Letters, 2021, 4, 22-25.	2.0	10
97	Race logic architecture (RALA): a novel logic concept using the race scheme of input variables. IEEE Journal of Solid-State Circuits, 2002, 37, 191-201.	5.4	9
98	Networks-on-chip and Networks-in-Package for High-Performance SoC Platforms. , 2005, , .		9
99	A 36.2 dB High SNR and PVT/Leakage-Robust eDRAM Computing-In-Memory Macro With Segmented BL and Reference Cell Array. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2433-2437.	3.0	9
100	A 120-mW 3-D rendering engine with 6-Mb embedded DRAM and 3.2-GB/s runtime reconfigurable bus for PDA chip. IEEE Journal of Solid-State Circuits, 2002, 37, 1352-1355.	5.4	8
101	The brain mimicking Visual Attention Engine: An 80×60 digital Cellular Neural Network for rapid global feature extraction. , 2008, , .		8
102	A low energy bio sensor node processor for continuous healthcare monitoring system. , 2008, , .		8
103	A multimodal drowsiness monitoring ear-module system with closed-loop real-time alarm. , 2016, , .		8
104	CNNP-v2:An Energy Efficient Memory-Centric Convolutional Neural Network Processor Architecture. , 2019, , .		8
105	A 4.45 ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices. , 2020, , .		8
106	A 9.6 mW/Ch 10 MHz Wide-bandwidth Electrical Impedance Tomography IC with Accurate Phase Compensation for Breast Cancer Detection. , 2020, , .		8
107	ECIM: Exponent Computing in Memory for an Energy-Efficient Heterogeneous Floating-Point DNN Training Processor. IEEE Micro, 2022, 42, 99-107.	1.8	8
108	An Arbitration Look-Ahead Scheme for Reducing End-to-End Latency in Networks on chip. , 0, , .		7

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109	A 152-mW Mobile Multimedia SoC With Fully Programmable 3-D Graphics and MPEG4/H.264/JPEG. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1260-1266.	3.1	7
110	A 20 µW contact impedance sensor for wireless body-area-network transceiver. , 2011, , .		7
111	A low energy crystal-less double-FSK transceiver for wireless body-area-network. , 2011, , .		7
112	An energy-efficient body channel communication based on Maxwell's equations analysis of on-body transmission mechanism. , 2012, , .		7
113	A 45μW injection-locked FSK Wake-Up receiver for crystal-less wireless body-area-network. , 2012, , .		7
114	A 4.9 mW neural network task scheduler for congestion-minimized network-on-chip in multi-core systems. , 2014, , .		7
115	A 0.5Â° Error 10 mW CMOS Image Sensor-Based Gaze Estimation Processor. IEEE Journal of Solid-State Circuits, 2016, 51, 1032-1040.	5.4	7
116	An energy-efficient deep learning processor with heterogeneous multi-core architecture for convolutional neural networks and recurrent neural networks. , 2017, , .		7
117	A 1GHz fault tolerant processor with dynamic lockstep and self-recovering cache for ADAS SoC complying with ISO26262 in automotive electronics. , 2017, , .		7
118	A 1.15 TOPS/W Energy-Efficient Capsule Network Accelerator for Real-Time 3D Point Cloud Segmentation in Mobile Environment. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1594-1598.	3.0	7
119	A 670 ps, 64 bit dynamic low-power adder design. , 0, , .		6
120	A multichip on oxide of 1 Gb/s 80 dB fully-differential CMOS transimpedance amplifier for optical interconnect applications. , 0, , .		6
121	Optimization of portable system architecture for real-time 3D graphics. , 0, , .		6
122	Intelligent NoC with neuro-fuzzy bandwidth regulation for a 51 IP object recognition processor. , 2010, , .		6
123	A 92m W 76.8GOPS vector matching processor with parallel Huffman decoder and query re-ordering buffer for real-time object recognition. , 2010, , .		6
124	A 92mW real-time traffic sign recognition system with robust light and dark adaptation. , 2011, , .		6
125	A 33μW/node Duty Cycle Controlled HBC Transceiver system for medical BAN with 64 sensor nodes. , 2014, , .		6
126	A 24-mW 28-Gb/s wireline receiver with low-frequency equalizing CTLE and 2-tap speculative DFE. , 2015, , .		6

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127	A Fault-Tolerant Cache System of Automotive Vision Processor Complying With ISO26262. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 1146-1150.	3.0	6
128	A 64.1mW Accurate Real-Time Visual Object Tracking Processor With Spatial Early Stopping on Siamese Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1675-1679.	3.0	6
129	DSPU: A 281.6mW Real-Time Depth Signal Processing Unit for Deep Learning-Based Dense RGB-D Data Acquisition with Depth Fusion and 3D Bounding Box Extraction in Mobile Platforms. , 2022, , .		6
130	An 1.61mW mixed-signal column processor for BRISK feature extraction in CMOS image sensor. , 2014, , .		5
131	An Energy-Efficient Deep Reinforcement Learning Accelerator With Transposable PE Array and Experience Compression. IEEE Solid-State Circuits Letters, 2019, 2, 228-231.	2.0	5
132	An 802.15.6 HBC Standard Compatible Transceiver and 90 pJ/b Full-Duplex Transceiver for Body Channel Communication. , 2019, , .		5
133	TSUNAMI: Triple Sparsity-Aware Ultra Energy-Efficient Neural Network Training Accelerator With Multi-Modal Iterative Pruning. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1494-1506.	5.4	5
134	480 ps 64-bit race logic adder. , 0, , .		4
135	A reconfigurable multilevel parallel texture cache memory with 75-GB/s parallel cache replacement bandwidth. IEEE Journal of Solid-State Circuits, 2002, 37, 612-623.	5.4	4
136	A 231MHz, 2.18mW 32-bit Logarithmic Arithmetic Unit for Fixed-Point 3D Graphics System. , 2005, , .		4
137	A 1.3pJ/b inductive coupling transceiver with adaptive gain control for Cm-range 50Mbps data communication. , 2009, , .		4
138	A 145µW 8×8 parallel multiplier based on optimized bypassing architecture. , 2011, , .		4
139	A 46 μW motion artifact reduction bio-signal sensor with ICA based adaptive DC level control for sleep monitoring system. , 2012, , .		4
140	A 43.7 mW 94 fps CMOS image sensor-based stereo matching accelerator with focal-plane rectification and analog census transformation. , 2016, , .		4
141	A CMOS Image Sensor-Based Stereo Matching Accelerator With Focal-Plane Sparse Rectification and Analog Census Transform. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 2180-2188.	5.4	4
142	Understanding Body Channel Communication : A review: from history to the future applications. , 2019, , .		4
143	A 15.2 TOPS/W CNN Accelerator with Similar Feature Skipping for Face Recognition in Mobile Devices. , 2019, , .		4
144	Direct Feedback Alignment Based Convolutional Neural Network Training for Low-Power Online Learning Processor. , 2019, , .		4

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145	An Energy-Efficient GAN Accelerator With On-Chip Training for Domain-Specific Optimization. IEEE Journal of Solid-State Circuits, 2021, 56, 2968-2980.	5.4	4
146	An 0.92 mJ/frame High-quality FHD Super-resolution Mobile Accelerator SoC with Hybrid-precision and Energy-efficient Cache. , 2022, , .		4
147	A compact ring delay line for high speed synchronous DRAM. , 0, , .		3
148	A low-noise folded bit-line sensing architecture for multigigabit DRAM with ultrahigh-density 6F/sup 2/ cell [CMOS design]. IEEE Journal of Solid-State Circuits, 1998, 33, 1096-1102.	5.4	3
149	A 76.8 GB/s 46 mW low-latency network-on-chip for real-time object recognition processor. , 2008, , .		3
150	A 1.5nJ/pixel super-resolution enhanced FAST corner detection processor for high accuracy AR. , 2014, , .		3
151	3.8 mW electrocardiogram (ECG) filtered electrical impedance tomography IC using I/Q homodyne architecture for breast cancer diagnosis. , 2014, , .		3
152	Intelligent task scheduler with high throughput NoC for real-time mobile object recognition SoC. , 2015, , .		3
153	79pJ/b 80Mb/s full-duplex transceiver and 42.5jW 100kb/s super-regenerative transceiver for body channel communication. , 2015, , .		3
154	A 635 $\frac{1}{4}$ W non-contact compensation IC for body channel communication. , 2016, , .		3
155	30-fps SNR equalized electrical impedance tomography IC with fast-settle filter and adaptive current control for lung monitoring. , 2016, , .		3
156	A 540- μ W Duty Controlled RSSI With Current Reusing Technique for Human Body Communication. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 893-901.	4.0	3
157	A fabric wrist patch sensor for continuous and comprehensive monitoring of the cardiovascular system. , 2016, 2016, 6070-6073.		3
158	A Capsule Endoscope System for Wide Visualization Field and Location Tracking. , 2018, , .		3
159	CNNP-v2: A Memory-Centric Architecture for Low-Power CNN Processor on Domain-Specific Mobile Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 598-611.	3.6	3
160	A 43.1TOPS/W Energy-Efficient Absolute-Difference-Accumulation Operation Computing-In-Memory With Computation Reuse. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1605-1609.	3.0	3
161	A Low-Power Graph Convolutional Network Processor With Sparse Grouping for 3D Point Cloud Semantic Segmentation in Mobile Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1507-1518.	5.4	3
162	AI SoCs for AR/VR User-Interaction. , 2021, , .		3

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163	Diffusion of zinc into gaas through Al _{0.3} Ga _{0.7} As. Journal of Electronic Materials, 1988, 17, 337-339.	2.2	2
164	POPeYE: a system analysis tool for DRAM performance measurement. , 0, , .		2
165	A 120 mW embedded 3D graphics rendering engine with 6 Mb logically local frame-buffer and 3.2 GByte/s run-time reconfigurable bus for PDA-chip. , 0, , .		2
166	A practical method to use eDRAM in the shared bus packet switch. , 0, , .		2
167	A Fixed-point 3D Graphics Library with Energy-efficient Cache Architecture for Mobile Multimedia Systems. , 0, , .		2
168	An Embedded 8-bit RISC Controller for Yield Enhancement of the 90-nm PRAM. , 2007, , .		2
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