Wolfgang Kunz

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/5559996/publications.pdf

Version: 2024-02-01

21 papers	183 citations	1684188 5 h-index	1720034 7 g-index
21 all docs	21 docs citations	21 times ranked	80 citing authors

#	Article	IF	Citations
1	Properties Firstâ€"Correct-By-Construction RTL Design in System-Level Design Flows. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3093-3106.	2.7	7
2	Automatic State Space Analysis for Modeling Untrusted Embedded Device Drivers. , 2020, , .		0
3	Processor Hardware Security Vulnerabilities and their Detection by Unique Program Execution Checking. , 2019, , .		22
4	Exploiting Hardware Unobservability for Low-Power Design and Safety Analysis in Formal Verification-Driven Design Flows. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1262-1275.	3.1	3
5	Systematic RISC-V based Firmware Designâ‹†. , 2019, , .		2
6	Generation of Abstract Driver Models for IP Integration Verification. IEEE Transactions on Emerging Topics in Computing, 2018, , 1-1.	4.6	1
7	Symbolic quick error detection using symbolic initial state for pre-silicon verification. , 2018, , .		9
8	A HW/SW Cross-Layer Approach for Determining Application-Redundant Hardware Faults in Embedded Systems. Journal of Electronic Testing: Theory and Applications (JETTA), 2017, 33, 77-92.	1.2	6
9	Dynamic Power Optimization Based on Formal Property Checking of Operations. , 2017, , .		1
10	goSAT: Floating-point satisfiability as global optimization. , 2017, , .		6
11	Safety across the HW/SW interface - Can formal methods meet the challenge?. , 2016, , .		0
12	A HW-dependent software model for cross-layer fault analysis in embedded systems. , 2016, , .		2
13	Architectural system modeling for correct-by-construction RTL design. , 2015, , .		2
14	Path Predicate Abstraction for Sound System-Level Models of RT-Level Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 291-304.	2.7	20
15	Formal system-on-chip verification: An operation-based methodology and its perspectives in low power design. , 2013, , .		0
16	A computational model for SAT-based verification of hardware-dependent low-level embedded system software. , 2013, , .		6
17	STABLE: A new QF-BV SMT solver for hard verification problems combining Boolean reasoning with computer algebra. , 2011, , .		30
18	Unbounded Protocol Compliance Verification Using Interval Property Checking With Invariants. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2068-2082.	2.7	47

#	Article	IF	Citations
19	Proving Functional Correctness of Weakly Programmable IPs - A Case Study with Formal Property Checking. , 2008, , .		7
20	A Normalization Method for Arithmetic Data-Path Verification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1909-1922.	2.7	12
21	Frontend model generation for SAT-based property checking. , 0, , .		0