Timothy Sherwood

List of Publications by Year
in descending order

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138	4,391	304368	344852
papers	citations	22 h-index	36 g-index

139	139	139	1718
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Automatically characterizing large scale program behavior. , 2002, , .		1,213
2	Phase tracking and prediction. , 2003, , .		209
3	Complete information flow tracking from the gates up. , 2009, , .		157
4	A High Throughput String Matching Architecture for Intrusion Detection and Prevention. Computer Architecture News, 2005, 33, 112-122.	2.5	150
5	A thermally-aware performance analysis of vertically integrated (3-D) processor-memory hierarchy. , 2006, , .		127
6	Sapper. , 2014, , .		83
7	Phase tracking and prediction. Computer Architecture News, 2003, 31, 336-349.	2.5	81
8	Using SimPoint for accurate and efficient simulation. Performance Evaluation Review, 2003, 31, 318-319.	0.4	80
9	Crafting a usable microkernel, processor, and I/O system with strict and provable information flow security. , 2011, , .		78
10	Reducing cache misses using hardware and software page placement. , 1999, , .		76
11	Automatically characterizing large scale program behavior. Computer Architecture News, 2002, 30, 45-57.	2.5	75
12	Preventing PCM banks from seizing too much power. , 2011, , .		75
13	Bit-split string-matching engines for intrusion detection and prevention. Transactions on Architecture and Code Optimization, 2006, 3, 3-34.	1.6	74
14	Ternary CAM Power and Delay Model: Extensions and Uses. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 554-564.	2.1	73
15	Moats and Drawbridges: An Isolation Primitive for Reconfigurable Hardware Based Systems. , 2007, , .		71
16	SurfNoC. , 2013, , .		68
17	Caisson. , 2011, , .		65
18	Execution leases. , 2009, , .		65

#	Article	IF	Citations
19	Automatically characterizing large scale program behavior. Operating Systems Review (ACM), 2002, 36, 45-57.	1.5	63
20	Automatically characterizing large scale program behavior. ACM SIGPLAN Notices, 2002, 37, 45-57.	0.2	60
21	A 3-D Split Manufacturing Approach to Trustworthy System Development. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 611-615.	1.9	53
22	DeepSniffer. , 2020, , .		51
23	Theoretical Fundamentals of Gate Level Information Flow Tracking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1128-1140.	1.9	49
24	Information flow isolation in I2C and USB. , 2011, , .		47
25	Managing Security in FPGA-Based Embedded Systems. IEEE Design and Test of Computers, 2008, 25, 590-598.	1.4	44
26	Data analysis on interactive whiteboards through sketch-based interaction. , 2011, , .		44
27	Leveraging Gate-Level Properties to Identify Hardware Timing Channels. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1288-1301.	1.9	39
28	Exploring the limits of leakage power reduction in caches. Transactions on Architecture and Code Optimization, 2005, 2, 221-246.	1.6	38
29	Reducing code size with echo instructions. , 2003, , .		37
30	Caisson. ACM SIGPLAN Notices, 2011, 46, 109-120.	0.2	37
31	Opportunities and Challenges of Using Plasmonic Components in Nanophotonic Architectures. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 154-168.	2.7	36
32	Handbook of FPGA Design Security. , 2010, , .		33
33	SurfNoC. Computer Architecture News, 2013, 41, 583-594.	2.5	33
34	A pythonic approach for rapid hardware prototyping and instrumentation. , 2017, , .		33
35	Networks on Chip with Provable Security Properties. IEEE Micro, 2014, 34, 57-68.	1.8	31
36	A Computational Temporal Logic for Superconducting Accelerators. , 2020, , .		31

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37	Hybrid CMOS/nanodevice circuits for high throughput pattern matching applications. , 2011, , .		30
38	Race Logic: A hardware acceleration for dynamic programming algorithms. , 2014, , .		30
39	Fighting fire with fire. , 2011, , .		29
40	Gate-Level Information Flow Tracking for Security Lattices. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-25.	1.9	29
41	On the Complexity of Generating Gate Level Information Flow Tracking Logic. IEEE Transactions on Information Forensics and Security, 2012, 7, 1067-1080.	4.5	28
42	A small cache of large ranges: Hardware methods for efficiently searching, storing, and updating big dataflow tags. , 2008, , .		27
43	Multi-execution. , 2009, , .		27
44	Exploring the Processor and ISA Design for Wireless Sensor Network Applications. , 2008, , .		25
45	Theoretical analysis of gate level information flow tracking. , 2010, , .		25
46	Complete information flow tracking from the gates up. ACM SIGPLAN Notices, 2009, 44, 109-120.	0.2	24
47	Understanding and visualizing full systems with data flow tomography. , 2008, , .		23
48	Enforcing memory policy specifications in reconfigurable hardware. Computers and Security, 2008, 27, 197-215.	4.0	22
49	Race logic. Computer Architecture News, 2014, 42, 517-528.	2.5	22
50	Protecting Page Tables from RowHammer Attacks using Monotonic Pointers in DRAM True-Cells. , 2019, , .		21
51	Memristors for neural branch prediction. , 2013, , .		18
52	Exploiting Data Similarity to Reduce Memory Footprints. , 2011, , .		16
53	Automated design of finite state machine predictors for customized processors. , 2001, , .		14
54	Inspection resistant memory. Computer Architecture News, 2012, 40, 130-141.	2.5	14

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55	Boosted Race Trees for Low Energy Classification. , 2019, , .		14
56	Agile Hardware Development and Instrumentation With PyRTL. IEEE Micro, 2020, 40, 76-84.	1.8	13
57	A Qualitative Security Analysis of a New Class of 3-D Integrated Crypto Co-processors. Lecture Notes in Computer Science, 2012, , 364-382.	1.0	13
58	SimPoint. , 2005, , 117-138.		13
59	Loop Termination Prediction. Lecture Notes in Computer Science, 2000, , 73-87.	1.0	12
60	Efficient remote profiling for resource-constrained devices. Transactions on Architecture and Code Optimization, 2006, 3, 35-66.	1.6	12
61	Hardware assistance for trustworthy systems through 3-D integration. , 2010, , .		12
62	Eliminating Timing Information Flows in a Mix-Trusted System-on-Chip. IEEE Design and Test, 2013, 30, 55-62.	1.1	12
63	Sapper. Computer Architecture News, 2014, 42, 97-112.	2.5	12
64	Security Primitives for Reconfigurable Hardware-Based Systems. ACM Transactions on Reconfigurable Technology and Systems, 2010, 3, 1-35.	1.9	11
65	A Practical Testing Framework for Isolating Hardware Timing Channels. , 2013, , .		11
66	Quantitative Analysis of Timing Channel Security in Cryptographic Hardware Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1719-1732.	1.9	11
67	Temporal Computing With Superconductors. IEEE Micro, 2021, 41, 71-79.	1.8	11
68	Leakage power reduction of embedded memories on FPGAs through location assignment. , 2006, , .		10
69	Crafting a usable microkernel, processor, and I/O system with strict and provable information flow security. Computer Architecture News, 2011, 39, 189-200.	2.5	10
70	Balancing design options with Sherpa. , 2004, , .		9
71	Gate-Level Information-Flow Tracking for Secure Architectures. IEEE Micro, 2010, 30, 92-100.	1.8	9
72	Quantifying timing-based information flow in cryptographic hardware. , 2015, , .		9

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73	Race Logic: Abusing Hardware Race Conditions to Perform Useful Computation. IEEE Micro, 2015, 35, 48-57.	1.8	9
74	Hiding Intermittent Information Leakage with Architectural Support for Blinking. , 2018, , .		9
75	High-Bandwidth Network Memory System Through Virtual Pipelines. IEEE/ACM Transactions on Networking, 2009, 17, 1029-1041.	2.6	8
76	Analysis of performance versus security in hardware realizations of small elliptic curves for lightweight applications. Journal of Cryptographic Engineering, 2012, 2, 179-188.	1.5	8
77	Secure information flow analysis for hardware design. , 2010, , .		8
78	Virtually Pipelined Network Memory. , 2006, , .		7
79	Quantifying the Potential of Program Analysis Peripherals. , 2009, , .		7
80	Estimating and understanding architectural risk. , 2017, , .		7
81	Superconducting Computing with Alternating Logic Elements. , 2021, , .		7
82	An Architecture Supporting Formal and Compositional Binary Analysis. , 2017, , .		6
83	A 4-mm2180-nm-CMOS 15-Giga-cell-updates-per-second DNA sequence alignment engine based on asynchronous race conditions. , 2017, , .		6
84	Automata-Theoretic Analysis of Bit-Split Languages for Packet Scanning. Lecture Notes in Computer Science, 2008, , 141-150.	1.0	6
85	Hardware trust implications of 3-D integration. , 2010, , .		6
86	A case study of multi-threading in the embedded space. , 2006, , .		6
87	Energy efficient computation with asynchronous races. , 2016, , .		5
88	Charm: A Language for Closed-Form High-Level Architecture Modeling. , 2018, , .		5
89	Safer Program Behavior Sharing Through Trace Wringing. , 2019, , .		5
90	Wire sorts: a language abstraction for safe hardware composition. , 2021, , .		5

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91	3D Integration for Introspection. IEEE Micro, 2007, 27, 77-83.	1.8	4
92	Extended abstract: Trustworthy system security through 3-D integrated hardware. , 2008, , .		4
93	Understanding and visualizing full systems with data flow tomography. ACM SIGPLAN Notices, 2008, 43, 211-221.	0.2	4
94	VrtProf: Vertical Profiling for System Virtualization. , 2010, , .		4
95	Efficient Uncertainty Modeling for System Design via Mixed Integer Programming. , 2019, , .		4
96	Towards understanding architectural tradeoffs in MEMS closed-loop feedback control. , 2007, , .		4
97	Sapper. ACM SIGPLAN Notices, 2014, 49, 97-112.	0.2	4
98	Automated design of finite state machine predictors for customized processors. Computer Architecture News, 2001, 29, 86-97.	2.5	3
99	Guiding Architectural SRAM Models. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	3
100	Understanding and visualizing full systems with data flow tomography. Operating Systems Review (ACM), 2008, 42, 211-221.	1.5	3
101	PSMalloc. , 2009, , .		3
102	Con?ict-Avoidance in Multicore Caching for Data-Similar Executions. , 2009, , .		3
103	PyRTL in Early Undergraduate Research. , 2019, , .		3
104	Inspection resistant memory: Architectural support for security from physical examination. , 2012, , .		2
105	Addressing the Challenges of Synchronization/Communication and Debugging Support in Hardware/Software Cosimulation. , 2008, , .		1
106	Whiteboards that compute: A workload analysis. , 2008, , .		1
107	Formulating and implementing profiling over adaptive ranges. Transactions on Architecture and Code Optimization, 2008, 5, 1-32.	1.6	1
108	ANALYSIS OF BIT-SPLIT LANGUAGES FOR PACKET SCANNING AND EXPERIMENTS WITH WILDCARD MATCHING. International Journal of Foundations of Computer Science, 2009, 20, 597-612.	0.8	1

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109	Position paper. , 2013, , .		1
110	Challenging on-chip SRAM security with boot-state statistics. , 2017, , .		1
111	An Architecture Supporting Formal and Compositional Binary Analysis. Computer Architecture News, 2017, 45, 177-191.	2.5	1
112	Thermal-aware, heterogeneous materials for improved energy and reliability in 3D PCM architectures. , 2017, , .		1
113	Architectural Risk. IEEE Micro, 2018, 38, 116-125.	1.8	1
114	Bouncer. , 2019, , .		1
115	PyRTLMatrix: An Object-Oriented Hardware Design Pattern for Prototyping ML Accelerators. , 2019, , .		1
116	In-sensor classification with boosted race trees. Communications of the ACM, 2021, 64, 99-105.	3.3	1
117	Extensible control architectures. , 2006, , .		1
118	Information Leakage in Arbiter Protocols. Lecture Notes in Computer Science, 2018, , 404-421.	1.0	1
119	Context-Aware Privacy-Optimizing Address Tracing. , 2021, , .		1
120	PyLSE: a pulse-transfer level language for superconductor electronics. , 2022, , .		1
121	Patchable instruction ROM architecture. , 2001, , .		0
122	Structural integrity. ACM SIGBED Review, 2008, 5, 1-2.	1.8	0
123	Metric Based Multi-Timescale Control for Reducing Power in Embedded Systems. , 2009, , .		0
124	Function flattening for lease-based, information-leak-free systems. , 2010, , .		0
125	Inspection-Resistant Memory Architectures. IEEE Micro, 2013, 33, 48-56.	1.8	0
126	An Architecture for Analysis. IEEE Micro, 2018, 38, 107-115.	1.8	0

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127	Language Support for Navigating Architecture Design in Closed Form. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-28.	1.8	0
128	Trace Wringing for Program Trace Privacy. IEEE Micro, 2020, , 1-1.	1.8	0
129	Safe functional systems through integrity types and verified assembly. Theoretical Computer Science, 2021, 851, 39-61.	0.5	0
130	ToolBlocks: An Infrastructure for the Construction of Memory Hierarchy Analysis Tools. Lecture Notes in Computer Science, 2000, , 70-74.	1.0	0
131	Metric Based Multi-Timescale Control for Reducing Power in Embedded Systems. Journal of Low Power Electronics, 2009, 5, 354-362.	0.6	0
132	Spatial Separation with Moats. , 2010, , 127-138.		0
133	Hardware Security Challenges. , 2010, , 71-85.		0
134	FPGA Updates and Programmability. , 2010, , 87-96.		0
135	Memory Protection on FPGAs. , 2010, , 97-126.		0
136	Representative Sampling Using SimPoint. , 2010, , 161-177.		0
137	Your Desktop or Mine: Extending the Reach of Writing Instruction. Ubiquitous Learning, 2011, 3, 129-140.	0.2	0
138	Hardware-Assisted Context Management for Accelerator Virtualization: A Case Study with RSA. Lecture Notes in Computer Science, 2016, , 72-83.	1.0	0