Anastasios Psarras

List of Publications by Year
in descending order

13	139	1307594 7	1588992 8
papers	citations	h-index	g-index

13	13	13	106
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	ShortPath: A Network-on-Chip Router with Fine-Grained Pipeline Bypassing. IEEE Transactions on Computers, 2016, 65, 3136-3147.	3.4	25
2	Microarchitecture of Network-on-Chip Routers. , 2015, , .		21
3	ElastiStore: Flexible Elastic Buffering for Virtual-Channel-Based Networks on Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3015-3028.	3.1	19
4	Networks-on-Chip With Double-Data-Rate Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3103-3114.	5.4	14
5	A Low-Power Network-on-Chip Architecture for Tile-based Chip Multi-Processors. , 2016, , .		13
6	PhaseNoC: Versatile Network Traffic Isolation Through TDM-Scheduled Virtual Channels. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 844-857.	2.7	13
7	Active Thermoelectric Cooling Solutions for Airspace Applications: the THERMICOOL Project. IEEE Access, 2017, 5, 2288-2299.	4.2	10
8	A Dual-Clock Multiple-Queue Shared Buffer. IEEE Transactions on Computers, 2017, 66, 1809-1815.	3.4	10
9	The Mesochronous Dual-Clock FIFO Buffer. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 302-306.	3.1	9
10	Simulation of the Dynamics of Bacterial Quorum Sensing. IEEE Transactions on Nanobioscience, 2015, 14, 440-446.	3.3	2
11	Timing-resilient Network-on-Chip architectures. , 2015, , .		1
12	RapidLink: A network-on-chip architecture with double-data-rate links. , 2016, , .		1
13	Low-power dual-edge-triggered synchronous latency-insensitive systems. , 2018, , .		1