Saumya Bhadauria

List of Publications by Year
in descending order

16 papers	205 citations	1684188 5 h-index	1474206 9 g-index
16 all docs	16 docs citations	16 times ranked	94 citing authors

#	Article	IF	Citations
1	TL-HLS: Methodology for Low Cost Hardware Trojan Security Aware Scheduling With Optimal Loop Unrolling Factor During High Level Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 655-668.	2.7	54
2	Exploring Low Cost Optimal Watermark for Reusable IP Cores During High Level Synthesis. IEEE Access, 2016, 4, 2198-2215.	4.2	50
3	Embedding low cost optimal watermark during high level synthesis for reusable IP core protection. , 2016, , .		18
4	Automated exploration of datapath in high level synthesis using temperature dependent bacterial foraging optimization algorithm. , 2014, , .		14
5	Bacterial foraging driven exploration of multi cycle fault tolerant datapath based on power-performance tradeoff in high level synthesis. Expert Systems With Applications, 2015, 42, 4719-4732.	7.6	14
6	Untrusted Third Party Digital IP Cores. , 2015, , .		14
7	Exploration of Multi-objective Tradeoff during High Level Synthesis Using Bacterial Chemotaxis and Dispersal. Procedia Computer Science, 2014, 35, 63-72.	2.0	11
8	Adaptive bacterial foraging driven datapath optimization: Exploring power-performance tradeoff in high level synthesis. Applied Mathematics and Computation, 2015, 269, 265-278.	2.2	10
9	User power-delay budget driven PSO based design space exploration of optimal k-cycle transient fault secured datapath during high level synthesis. , 2015, , .		6
10	Lowâ€cost security aware HLS methodology. IET Computers and Digital Techniques, 2017, 11, 68-79.	1.2	4
11	Watermarking of Deep Recurrent Neural Network Using Adversarial Examples to Protect Intellectual Property. Applied Artificial Intelligence, 2022, 36, .	3.2	4
12	Low cost optimized Trojan secured schedule at behavioral level for single & Nested loop control data flow graphs (Invited Paper). The Integration VLSI Journal, 2017, 58, 378-389.	2.1	3
13	Error Masking of Transient Faults: Exploration of a Fault Tolerant Datapath Based on User Specified Power and Delay Budget. , 2014, , .		1
14	Secure Information Processing during System-Level: Exploration of an Optimized Trojan Secured Datapath for CDFGs during HLS Based on User Constraints. , 2015, , .		1
15	Automated design space exploration of multi-cycle transient fault detectable datapath based on multi-objective user constraints for application specific computing. Advances in Engineering Software, 2015, 82, 14-24.	3.8	1
16	Automated design space exploration of transient fault detectable datapath based on user specified power and delay constraints. , 2015, , .		0