Rajesh K Gupta

List of Publications by Year in Descending Order

38 papers	885 citations	16 h-index	29 g-index
45 ext. papers	1,137 ext. citations	3.5 avg, IF	4.29 L-index

#	Paper	IF	Citations
38	Hardware/Software Codesign for Energy Efficiency and Robustness: From Error-Tolerant Computing to Approximate Computing. *Embedded Systems*, **2021**, 527-543		2
37	Performance Analysis of Timing-Speculative Processors. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	0
36	Critical Risk Indicators (CRIs) for the electric power grid: a survey and discussion of interconnected effects. *Environment Systems and Decisions*, **2021**, 1-22	4.1	2
35	ACES. *ACM Transactions on Sensor Networks*, **2020**, 16, 1-31	2.9	4
34	Formalizing Tag-Based Metadata With the Brick Ontology. *Frontiers in Built Environment*, **2020**, 6,	2.2	7
33	Accelerating Local Binary Pattern Networks with Software-Programmable FPGAs **2019**,		4
32	Serving deep neural networks at the cloud edge for vision applications on mobile platforms **2019**,		5
31	Variability Expeditions: A Retrospective. *IEEE Design and Test*, **2019**, 36, 65-67	1.4	2
30	A Wearable, Extensible, Open-Source Platform for Hearing Healthcare Research. *IEEE Access*, **2019**, 7, 162083-162101	3.5	7
29	Beyond a House of Sticks **2019**,		4
28	Multi-tenant mobile offloading systems for real-time computer vision applications **2019**,		5
27	Brick : Metadata schema for portable smart building applications. *Applied Energy*, **2018**, 226, 1273-1292	10.7	60
26	CLIM: A Cross-Level Workload-Aware Timing Error Prediction Model for Functional Units. *IEEE Transactions on Computers*, **2018**, 67, 771-783	2.5	16
25	Energy-efficient neural networks using approximate computation reuse **2018**,		22
24	SnaPEA: Predictive Early Activation for Reducing Computation in Deep Convolutional Neural Networks **2018**,		60
23	Mitigating Multi-tenant Interference in Continuous Mobile Offloading. *Lecture Notes in Computer Science*, **2018**, 20-36	0.9	1
22	SLoT: A supervised learning model to predict dynamic timing errors of functional units **2017**,		15

21	QoS-Aware Scheduling of Heterogeneous Servers for Inference in Deep Neural Networks **2017**,		16
20	Binarized Convolutional Neural Networks with Separable Filters for Efficient Hardware Acceleration **2017**,		11
19	Mitigating multi-tenant interference on mobile offloading servers **2017**,		1
18	Spatial and Temporal Memoization **2017**, 181-190		
17	CIRCA-GPUs: Increasing Instruction Reuse Through Inexact Computing in GP-GPUs. *IEEE Design and Test*, **2016**, 33, 85-92	1.4	6
16	. *Proceedings of the IEEE*, **2016**, 104, 1410-1448	14.3	25
15	Associative Memristive Memory for Approximate Computing in GPUs. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2016**, 6, 222-234	5.2	16
14	Supervised learning based model for predicting variability-induced timing errors **2015**,		6
13	Application-Adaptive Guardbanding to Mitigate Static and Dynamic Variability. *IEEE Transactions on Computers*, **2014**, 63, 2160-2173	2.5	26
12	Improving Resilience to Timing Errors by Exposing Variability Effects to Software in Tightly-Coupled Processor Clusters. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2014**, 4, 216-229	5.2	5
11	A variability-aware OpenMP environment for efficient execution of accuracy-configurable computation on shared-FPU processor clusters **2013**,		15
10	Spatial Memoization: Concurrent Instruction Reuse to Correct Timing Errors in SIMD Architectures. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 847-851	3.5	28
9	Underdesigned and Opportunistic Computing in Presence of Hardware Variability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 8-23	2.5	88
8	Analysis of instruction-level vulnerability to dynamic voltage and temperature variations **2012**,		18
7	Sensor localization with deterministic accuracy guarantee **2011**,		19
6	Underdesigned and Opportunistic Computing **2011**,		1
5	Understanding the Impact of Emerging Non-Volatile Memories on High-Performance, IO-Intensive Computing **2010**,		80
4	Optimal Speed Control of Mobile Node for Data Collection in Sensor Networks. *IEEE Transactions on Mobile Computing*, **2010**, 9, 127-139	4.6	106

3	Moneta: A High-Performance Storage Array Architecture for Next-Generation, Non-volatile Memories **2010**,		163
2	Translation Validation of High-Level Synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 566-579	2.5	35
1	Synthesis and Optimization of Combinational Interface Circuits. *Journal of Signal Processing Systems* , **2002**, 31, 243-261		1