

Shuang Zhu

List of Publications by Year in descending order

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papers

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#	ARTICLE	IF	CITATIONS
1	A 9-bit 215 MS/s Folding-Flash Time-to-Digital Converter Based on Redundant Remainder Number System in 45-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 839-849.	5.4	19
2	A 2-GS/s 8-bit Non-Interleaved Time-Domain Flash ADC Based on Remainder Number System in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 1172-1183.	5.4	47
3	Real-time Activity and Fall Risk Detection for Aging Population Using Deep Learning. , 2018, , .		12
4	A 2GS/s 8b flash ADC based on remainder number system in 65nm CMOS. , 2017, , .		9
5	A Skew-Free 10 GS/s 6 bit CMOS ADC With Compact Time-Domain Signal Folding and Inherent DEM. IEEE Journal of Solid-State Circuits, 2016, 51, 1785-1796.	5.4	54
6	A 24.7 mW 65 nm CMOS SAR-Assisted CT $\Delta\Sigma$ Modulator With Second-Order Noise Coupling Achieving 45 MHz Bandwidth and 75.3 dB SNDR. IEEE Journal of Solid-State Circuits, 2016, 51, 2893-2905.	5.4	32
7	A smart ECG sensor with in-situ adaptive motion-artifact compensation for dry-contact wearable healthcare devices. , 2016, , .		1
8	A 10-bit 250 MSPS charge-domain pipelined ADC with replica controlled PVT insensitive BCT circuit. Journal of Semiconductors, 2015, 36, 055012.	3.7	3
9	A 0.073-mm ² ; 10-GS/s 6-bit time-domain folding ADC in 65-nm CMOS with inherent DEM. , 2015, , .		4
10	A motion-artifact tracking and compensation technique for dry-contact EEG monitoring system. , 2014, , .		9
11	A 9-bit 215-MS/s folding-flash time-to-digital converter based on redundant remainder number system. , 2014, , .		8
12	A PVT insensitive BCT circuit with replica calibration for high speed charge-domain pipelined ADCs. , 2012, , .		1