Marco Lanuzza

List of Publications by Year in Descending Order

101 papers	1,042 citations	17 h-index	27 g-index
130 ext. papers	1,441 ext. citations	2.3 avg, IF	4.62 L-index

#	Paper	IF	Citations
101	Static CMOS Physically Unclonable Function Based on 4T Voltage Divider With 0.6%-1.5% Bit Instability at 0.4-1.8 V Operation in 180 nm. *IEEE Journal of Solid-State Circuits*, **2022**, 1-12	5.5	3
100	Hamming Distance Tolerant Content-Addressable Memory (HD-CAM) for DNA Classification. *IEEE Access*, **2022**, 10, 28080-28093	3.5	3
99	Embedded Memories for Cryogenic Applications. *Electronics (Switzerland)*, **2022**, 11, 61	2.6	3
98	Adjusting thermal stability in double-barrier MTJ for energy improvement in cryogenic STT-MRAMs. *Solid-State Electronics*, **2022**, 194, 108315	1.7	
97	A 0.6V–1.8V Compact Temperature Sensor with 0.24 °C Resolution, ±1.4 °C Inaccuracy and 1.06 nJ per Conversion. *IEEE Sensors Journal*, **2022**, 1-1	4	0
96	Smart Material Implication Using Spin-Transfer Torque Magnetic Tunnel Junctions for Logic-in-Memory Computing. *Solid-State Electronics*, **2022**, 108390	1.7	
95	Assessment of paper-based MoS2 FET for Physically Unclonable Functions. *Solid-State Electronics*, **2022**, 194, 108391	1.7	1
94	Field-Free Magnetic Tunnel Junction for Logic Operations Based on Voltage-Controlled Magnetic Anisotropy. *IEEE Magnetics Letters*, **2021**, 12, 1-4	1.6	0
93	A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1393-1397	3.5	1
92	A Low-Voltage, Low-Power Reconfigurable Current-Mode Softmax Circuit for Analog Neural Networks. *Electronics (Switzerland)*, **2021**, 10, 1004	2.6	2
91	Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures. *IEEE Transactions on Magnetics*, **2021**, 57, 1-6	2	9
90	An MTJ-Based Asynchronous System With Extremely Fine-Grained Voltage Scaling. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 311-321	3.9	
89	Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications. *IEEE Nanotechnology Magazine*, **2021**, 20, 123-128	2.6	11
88	A 0.05 mm2, 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	3
87	Ultralow Voltage FinFET- Versus TFET-Based STT-MRAM Cells for IoT Applications. *Electronics (Switzerland)*, **2021**, 10, 1756	2.6	4
86	Gain-Cell Embedded DRAM Under Cryogenic Operation—A First Study. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 1319-1324	2.6	7
85	A 0.6-to-1.8V CMOS Current Reference With Near-100% Power Utilization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 3038-3042	3.5	3

84	Relaxing non-volatility for energy-efficient DMTJ based cryogenic STT-MRAM. *Solid-State Electronics*, **2021**, 184, 108090	1.7	7
83	Quantum capacitance transient phenomena in high-k dielectric armchair graphene nanoribbon field-effect transistor model. *Solid-State Electronics*, **2021**, 184, 108060	1.7	
82	Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 3134-3144	5.5	9
81	STT-MTJ Based Smart Implication for Energy-Efficient Logic-in-Memory Computing. *Solid-State Electronics*, **2021**, 184, 108065	1.7	3
80	Assessment of 2D-FET Based Digital and Analog Circuits on Paper. *Solid-State Electronics*, **2021**, 185, 108063	1.7	1
79	Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework. *The Integration VLSI Journal*, **2020**, 71, 56-69	1.4	11
78	Impact of Scaling on Physical Unclonable Function Based on Spin□Orbit Torque. *IEEE Magnetics Letters*, **2020**, 11, 1-5	1.6	1
77	A 0.8-V, 1.54-pJ/940-MHz Dual-Mode Logic-Based 16□16-b Booth Multiplier in 16-nm FinFET. *IEEE Solid-State Circuits Letters*, **2020**, 3, 314-317	2	5
76	Spin□rbit torque based physical unclonable function. *Journal of Applied Physics*, **2020**, 128, 033904	2.5	19
75	Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1639-1643	3.5	4
74	Compact Modeling of Perpendicular STT-MTJs With Double Reference Layers. *IEEE Nanotechnology Magazine*, **2019**, 18, 1063-1070	2.6	13
73	Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. *Microelectronic Engineering*, **2019**, 215, 111009	2.5	15
72	Double-precision Dual Mode Logic carry-save multiplier. *The Integration VLSI Journal*, **2019**, 64, 71-77	1.4	0
71	Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs **2019**,		3
70	Making IoT Services Accountable: A Solution Based on Blockchain and Physically Unclonable Functions. *Lecture Notes in Computer Science*, **2019**, 294-305	0.9	2
69	An Energy Aware Variation-Tolerant Writing Termination Control for STT-based Non Volatile Flip-Flops **2019**,		1
68	An 88-fJ/40-MHz [0.4 V]□0.61-pJ/1-GHz [0.9 V] Dual-Mode Logic 8 $times$ 8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 560-568	5.5	15
67	A portable class of 3-transistor current references with low-power sub-0.5□V operation. *International Journal of Circuit Theory and Applications*, **2018**, 46, 779-795	2	7

66	A Variation-Aware Timing Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 1086-1095	3.9	26
65	Digital and analog TFET circuits: Design and benchmark. *Solid-State Electronics*, **2018**, 146, 50-65	1.7	40
64	An Ultralow-Voltage Energy-Efficient Level Shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 61-65	3.5	38
63	Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. *Progress in Photovoltaics: Research and Applications*, **2017**, 25, 452-469	6.8	27
62	Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits. *IEEE Transactions on Electron Devices*, **2017**, 64, 2736-2743	2.9	39
61	Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework. *IEEE Nanotechnology Magazine*, **2017**, 16, 160-168	2.6	22
60	Understanding the impact of point-contact scheme and selective emitter in a c-Si BC-BJ solar cell by full 3D numerical simulations. *Solar Energy*, **2017**, 155, 1443-1450	6.8	1
59	A variation-aware simulation framework for hybrid CMOS/spintronic circuits **2017**,		3
58	Impact of voltage scaling on STT-MRAMs through a variability-aware simulation framework **2017**,		4
57	Benchmarks of a III-V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits. *Solid-State Electronics*, **2017**, 128, 37-42	1.7	12
56	A physical unclonable function based on a 2-transistor subthreshold voltage divider. *International Journal of Circuit Theory and Applications*, **2017**, 45, 260-273	2	7
55	Low energy/delay overhead level shifter for wide-range voltage conversion. *International Journal of Circuit Theory and Applications*, **2017**, 45, 1637-1646	2	3
54	Evaluation of Dual Mode Logic in 28nm FD-SOI technology **2017**,		3
53	A Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs. *IEEE Transactions on Electron Devices*, **2017**, 64, 4346-4353	2.9	26
52	Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. *IEEE Transactions on Electron Devices*, **2016**, 63, 2749-2756	2.9	33
51	Low voltage logic circuits exploiting gate level dynamic body biasing in 28 nm UTBB FD-SOI. *Solid-State Electronics*, **2016**, 117, 185-192	1.7	27
50	Benchmarks of a III-V TFET technology platform against the 10-nm CMOS technology node considering 28T Full-Adders **2016**,		1
49	Design guidelines for a metallization scheme with multiple-emitter contact lines in BC-BJ solar cells. *Journal of Computational Electronics*, **2016**, 15, 1498-1504	1.8	1

48	Extended exploration of low granularity back biasing control in 28nm UTBB FD-SOI technology **2016**,		3
47	Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain. *IEEE Transactions on Electron Devices*, **2015**, 62, 3973-3979	2.9	47
46	Gate-level body biasing for subthreshold logic circuits: analytical modeling and design guidelines. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1523-1540	2	7
45	Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 388-391	2.6	47
44	Skyrmion based microwave detectors and harvesting. *Applied Physics Letters*, **2015**, 107, 262401	3.4	64
43	Ultra-Low-Voltage Self-Body Biasing Scheme and Its Application to Basic Arithmetic Circuits. *VLSI Design*, **2015**, 2015, 1-10		5
42	Low voltage ripple carry adder with low-granularity dynamic forward back-biasing in 28 nm UTBB FD-SOI **2015**,		1
41	Improving speed and power characteristics of pulse-triggered flip-flops **2014**,		2
40	Designing Dynamic Carry Skip Adders: Analysis and Comparison. *Circuits, Systems, and Signal Processing*, **2014**, 33, 1019-1034	2.2	1
39	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 1456-1464	3.9	16
38	Dynamic gate-level body biasing for subthreshold digital design **2014**,		9
37	Exploring back biasing opportunities in 28nm UTBB FD-SOI technology for subthreshold digital design **2014**,		6
36	Design of high-speed low-power parallel-prefix adder trees in nanometer technologies. *International Journal of Circuit Theory and Applications*, **2014**, 42, 731-743	2	4
35	Analyzing noise robustness of wide fan-in dynamic logic gates under process variations. *International Journal of Circuit Theory and Applications*, **2014**, 42, 452-467	2	2
34	Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates. *International Journal of Circuit Theory and Applications*, **2014**, 42, 65-70	2	32
33	A Comparative Study of MWT Architectures by Means of Numerical Simulations. *Energy Procedia*, **2013**, 38, 131-136	2.3	1
32	A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops. *Journal of Low Power Electronics*, **2013**, 9, 445-451	1.2	3
31	Energy-efficient single-clock-cycle binary comparator. *International Journal of Circuit Theory and Applications*, **2012**, 40, 237-246	2	9

30	Low-Power Level Shifter for Multi-Supply Voltage Designs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 922-926	3.5	54
29	Optimization of Rear Point Contact Geometry by Means of 3-D Numerical Simulation. *Energy Procedia*, **2012**, 27, 197-202	2.3	9
28	Comparative analysis of yield optimized pulsed flip-flops. *Microelectronics Reliability*, **2012**, 52, 1679-1689	2.2	20
27	Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. *Journal of Low Power Electronics and Applications*, **2011**, 1, 97-108	1.7	7
26	Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis. *Lecture Notes in Computer Science*, **2011**, 180-189	0.9	5
25	A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs **2010**,		9
24	Exploiting Self-Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications. *ACM Transactions on Reconfigurable Technology and Systems*, **2010**, 4, 1-22	2.7	8
23	A new low-power high-speed single-clock-cycle binary comparator **2010**,		7
22	Impact of Process Variations on Flip-Flops Energy and Timing Characteristics **2010**,		13
21	Design Space Exploration of Split-Path Data Driven Dynamic Full Adder. *Journal of Low Power Electronics*, **2010**, 6, 469-481	1.2	4
20	A New Optimized High-Speed Low-Power Data-Driven Dynamic (D3L) 32-Bit Kogge-Stone Adder. *Lecture Notes in Computer Science*, **2010**, 357-366	0.9	2
19	An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. *Lecture Notes in Computer Science*, **2009**, 74-84	0.9	4
18	Low-power split-path data-driven dynamic logic. *IET Circuits, Devices and Systems*, **2009**, 3, 303-312	1.1	12
17	Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath **2009**,		7
16	New performance/power/area efficient, reliable full adder design **2009**,		6
15	Designing High-Speed Adders in Power-Constrained Environments. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 172-176	3.5	17
14	A novel ICA-based hardware system for reconfigurable and portable BCI **2009**,		7
13	Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. *Journal of Low Power Electronics*, **2009**, 5, 326-338	1.2	6

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12	Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. *Lecture Notes in Computer Science*, **2009**, 297-306	0.9	
11	Performance and reliability of ultra-thin oxide nMOSFETs under variable body bias. *Microelectronic Engineering*, **2007**, 84, 1947-1950	2.5	2
10	A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications **2007**,		14
9	MORA: A New Coarse-Grain Reconfigurable Array for High Throughput Multimedia Processing **2007** , 159-168		11
8	Low bit rate image compression core for onboard space applications. *IEEE Transactions on Circuits and Systems for Video Technology*, **2006**, 16, 114-128	6.4	15
7	A high-performance fully reconfigurable FPGA-based 2D convolution processor. *Microprocessors and Microsystems*, **2005**, 29, 381-391	2.4	28
6	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications **2005**,		6
5	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications **2005**,		5
4	Variable precision arithmetic circuits for FPGA-based multimedia processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2004**, 12, 995-999	2.6	9
3	An efficient wavelet image encoder for FPGA-based designs		4
2	Low-cost fully reconfigurable data-path for FPGA-based multimedia processor		1
1	Emerging Memory Structures for VLSI Circuits1-28		