

# Marco Lanuzza

## List of Publications by Citations

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

101  
papers

1,042  
citations

17  
h-index

27  
g-index

130  
ext. papers

1,441  
ext. citations

2.3  
avg, IF

4.62  
L-index

#	Paper	IF	Citations
101	Skyrmion based microwave detectors and harvesting. <i>Applied Physics Letters</i> , <b>2015</b> , 107, 262401	3.4	64
100	Low-Power Level Shifter for Multi-Supply Voltage Designs. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2012</b> , 59, 922-926	3.5	54
99	Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain. <i>IEEE Transactions on Electron Devices</i> , <b>2015</b> , 62, 3973-3979	2.9	47
98	Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2015</b> , 23, 388-391	2.6	47
97	Digital and analog TFET circuits: Design and benchmark. <i>Solid-State Electronics</i> , <b>2018</b> , 146, 50-65	1.7	40
96	Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits. <i>IEEE Transactions on Electron Devices</i> , <b>2017</b> , 64, 2736-2743	2.9	39
95	An Ultralow-Voltage Energy-Efficient Level Shifter. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2017</b> , 64, 61-65	3.5	38
94	Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. <i>IEEE Transactions on Electron Devices</i> , <b>2016</b> , 63, 2749-2756	2.9	33
93	Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates. <i>International Journal of Circuit Theory and Applications</i> , <b>2014</b> , 42, 65-70	2	32
92	A high-performance fully reconfigurable FPGA-based 2D convolution processor. <i>Microprocessors and Microsystems</i> , <b>2005</b> , 29, 381-391	2.4	28
91	Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. <i>Progress in Photovoltaics: Research and Applications</i> , <b>2017</b> , 25, 452-469	6.8	27
90	Low voltage logic circuits exploiting gate level dynamic body biasing in 28 nm UTBB FD-SOI. <i>Solid-State Electronics</i> , <b>2016</b> , 117, 185-192	1.7	27
89	A Variation-Aware Timing Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2018</b> , 65, 1086-1095	3.9	26
88	A Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs. <i>IEEE Transactions on Electron Devices</i> , <b>2017</b> , 64, 4346-4353	2.9	26
87	Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework. <i>IEEE Nanotechnology Magazine</i> , <b>2017</b> , 16, 160-168	2.6	22
86	Comparative analysis of yield optimized pulsed flip-flops. <i>Microelectronics Reliability</i> , <b>2012</b> , 52, 1679-1689	2	20
85	Spin-orbit torque based physical unclonable function. <i>Journal of Applied Physics</i> , <b>2020</b> , 128, 033904	2.5	19

84	Designing High-Speed Adders in Power-Constrained Environments. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2009</b> , 56, 172-176	3.5	17
83	. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2014</b> , 61, 1456-1464	3.9	16
82	Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. <i>Microelectronic Engineering</i> , <b>2019</b> , 215, 111009	2.5	15
81	Low bit rate image compression core for onboard space applications. <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , <b>2006</b> , 16, 114-128	6.4	15
80	An 88-fJ/40-MHz [0.4 V] 0.61-pJ/1-GHz [0.9 V] Dual-Mode Logic 8 $\times$ 8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI. <i>IEEE Journal of Solid-State Circuits</i> , <b>2019</b> , 54, 560-568	5.5	15
79	A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications <b>2007</b> ,		14
78	Compact Modeling of Perpendicular STT-MTJs With Double Reference Layers. <i>IEEE Nanotechnology Magazine</i> , <b>2019</b> , 18, 1063-1070	2.6	13
77	Impact of Process Variations on Flip-Flops Energy and Timing Characteristics <b>2010</b> ,		13
76	Benchmarks of a III-V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits. <i>Solid-State Electronics</i> , <b>2017</b> , 128, 37-42	1.7	12
75	Low-power split-path data-driven dynamic logic. <i>IET Circuits, Devices and Systems</i> , <b>2009</b> , 3, 303-312	1.1	12
74	Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework. <i>The Integration VLSI Journal</i> , <b>2020</b> , 71, 56-69	1.4	11
73	MORA: A New Coarse-Grain Reconfigurable Array for High Throughput Multimedia Processing <b>2007</b> , 159-168		11
72	Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications. <i>IEEE Nanotechnology Magazine</i> , <b>2021</b> , 20, 123-128	2.6	11
71	Dynamic gate-level body biasing for subthreshold digital design <b>2014</b> ,		9
70	Energy-efficient single-clock-cycle binary comparator. <i>International Journal of Circuit Theory and Applications</i> , <b>2012</b> , 40, 237-246	2	9
69	Optimization of Rear Point Contact Geometry by Means of 3-D Numerical Simulation. <i>Energy Procedia</i> , <b>2012</b> , 27, 197-202	2.3	9
68	A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs <b>2010</b> ,		9
67	Variable precision arithmetic circuits for FPGA-based multimedia processors. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2004</b> , 12, 995-999	2.6	9

66	Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures. <i>IEEE Transactions on Magnetics</i> , <b>2021</b> , 57, 1-6	2	9
65	Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. <i>IEEE Journal of Solid-State Circuits</i> , <b>2021</b> , 56, 3134-3144	5.5	9
64	Exploiting Self-Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications. <i>ACM Transactions on Reconfigurable Technology and Systems</i> , <b>2010</b> , 4, 1-22	2.7	8
63	Gate-level body biasing for subthreshold logic circuits: analytical modeling and design guidelines. <i>International Journal of Circuit Theory and Applications</i> , <b>2015</b> , 43, 1523-1540	2	7
62	A portable class of 3-transistor current references with low-power sub-0.5V operation. <i>International Journal of Circuit Theory and Applications</i> , <b>2018</b> , 46, 779-795	2	7
61	A physical unclonable function based on a 2-transistor subthreshold voltage divider. <i>International Journal of Circuit Theory and Applications</i> , <b>2017</b> , 45, 260-273	2	7
60	Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. <i>Journal of Low Power Electronics and Applications</i> , <b>2011</b> , 1, 97-108	1.7	7
59	A new low-power high-speed single-clock-cycle binary comparator <b>2010</b> ,		7
58	Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath <b>2009</b> ,		7
57	A novel ICA-based hardware system for reconfigurable and portable BCI <b>2009</b> ,		7
56	Gain-Cell Embedded DRAM Under Cryogenic Operation—A First Study. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2021</b> , 29, 1319-1324	2.6	7
55	Relaxing non-volatility for energy-efficient DMTJ based cryogenic STT-MRAM. <i>Solid-State Electronics</i> , <b>2021</b> , 184, 108090	1.7	7
54	Exploring back biasing opportunities in 28nm UTBB FD-SOI technology for subthreshold digital design <b>2014</b> ,		6
53	New performance/power/area efficient, reliable full adder design <b>2009</b> ,		6
52	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications <b>2005</b> ,		6
51	Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. <i>Journal of Low Power Electronics</i> , <b>2009</b> , 5, 326-338	1.2	6
50	Ultra-Low-Voltage Self-Body Biasing Scheme and Its Application to Basic Arithmetic Circuits. <i>VLSI Design</i> , <b>2015</b> , 2015, 1-10		5
49	Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis. <i>Lecture Notes in Computer Science</i> , <b>2011</b> , 180-189	0.9	5

48	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications <b>2005</b> ,		5
47	A 0.8-V, 1.54-pJ/940-MHz Dual-Mode Logic-Based 16 $\times$ 16-b Booth Multiplier in 16-nm FinFET. <i>IEEE Solid-State Circuits Letters</i> , <b>2020</b> , 3, 314-317	2	5
46	Impact of voltage scaling on STT-MRAMs through a variability-aware simulation framework <b>2017</b> ,		4
45	Design of high-speed low-power parallel-prefix adder trees in nanometer technologies. <i>International Journal of Circuit Theory and Applications</i> , <b>2014</b> , 42, 731-743	2	4
44	An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. <i>Lecture Notes in Computer Science</i> , <b>2009</b> , 74-84	0.9	4
43	An efficient wavelet image encoder for FPGA-based designs		4
42	Design Space Exploration of Split-Path Data Driven Dynamic Full Adder. <i>Journal of Low Power Electronics</i> , <b>2010</b> , 6, 469-481	1.2	4
41	Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2020</b> , 67, 1639-1643	3.5	4
40	Ultralow Voltage FinFET- Versus TFET-Based STT-MRAM Cells for IoT Applications. <i>Electronics (Switzerland)</i> , <b>2021</b> , 10, 1756	2.6	4
39	A variation-aware simulation framework for hybrid CMOS/spintronic circuits <b>2017</b> ,		3
38	Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs <b>2019</b> ,		3
37	Low energy/delay overhead level shifter for wide-range voltage conversion. <i>International Journal of Circuit Theory and Applications</i> , <b>2017</b> , 45, 1637-1646	2	3
36	Evaluation of Dual Mode Logic in 28nm FD-SOI technology <b>2017</b> ,		3
35	A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops. <i>Journal of Low Power Electronics</i> , <b>2013</b> , 9, 445-451	1.2	3
34	Extended exploration of low granularity back biasing control in 28nm UTBB FD-SOI technology <b>2016</b> ,		3
33	A 0.05 mm <sup>2</sup> , 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2021</b> , 1-1	3.5	3
32	A 0.6-to-1.8V CMOS Current Reference With Near-100% Power Utilization. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2021</b> , 68, 3038-3042	3.5	3
31	STT-MTJ Based Smart Implication for Energy-Efficient Logic-in-Memory Computing. <i>Solid-State Electronics</i> , <b>2021</b> , 184, 108065	1.7	3

30	Static CMOS Physically Unclonable Function Based on 4T Voltage Divider With 0.6%-1.5% Bit Instability at 0.4-1.8 V Operation in 180 nm. <i>IEEE Journal of Solid-State Circuits</i> , <b>2022</b> , 1-12	5.5	3
29	Hamming Distance Tolerant Content-Addressable Memory (HD-CAM) for DNA Classification. <i>IEEE Access</i> , <b>2022</b> , 10, 28080-28093	3.5	3
28	Embedded Memories for Cryogenic Applications. <i>Electronics (Switzerland)</i> , <b>2022</b> , 11, 61	2.6	3
27	Improving speed and power characteristics of pulse-triggered flip-flops <b>2014</b> ,		2
26	Analyzing noise robustness of wide fan-in dynamic logic gates under process variations. <i>International Journal of Circuit Theory and Applications</i> , <b>2014</b> , 42, 452-467	2	2
25	Performance and reliability of ultra-thin oxide nMOSFETs under variable body bias. <i>Microelectronic Engineering</i> , <b>2007</b> , 84, 1947-1950	2.5	2
24	Making IoT Services Accountable: A Solution Based on Blockchain and Physically Unclonable Functions. <i>Lecture Notes in Computer Science</i> , <b>2019</b> , 294-305	0.9	2
23	A New Optimized High-Speed Low-Power Data-Driven Dynamic (D3L) 32-Bit Kogge-Stone Adder. <i>Lecture Notes in Computer Science</i> , <b>2010</b> , 357-366	0.9	2
22	A Low-Voltage, Low-Power Reconfigurable Current-Mode Softmax Circuit for Analog Neural Networks. <i>Electronics (Switzerland)</i> , <b>2021</b> , 10, 1004	2.6	2
21	Understanding the impact of point-contact scheme and selective emitter in a c-Si BC-BJ solar cell by full 3D numerical simulations. <i>Solar Energy</i> , <b>2017</b> , 155, 1443-1450	6.8	1
20	Designing Dynamic Carry Skip Adders: Analysis and Comparison. <i>Circuits, Systems, and Signal Processing</i> , <b>2014</b> , 33, 1019-1034	2.2	1
19	A Comparative Study of MWT Architectures by Means of Numerical Simulations. <i>Energy Procedia</i> , <b>2013</b> , 38, 131-136	2.3	1
18	Low voltage ripple carry adder with low-granularity dynamic forward back-biasing in 28 nm UTBB FD-SOI <b>2015</b> ,		1
17	Low-cost fully reconfigurable data-path for FPGA-based multimedia processor		1
16	Impact of Scaling on Physical Unclonable Function Based on SpinOrbit Torque. <i>IEEE Magnetics Letters</i> , <b>2020</b> , 11, 1-5	1.6	1
15	A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2021</b> , 68, 1393-1397	3.5	1
14	Benchmarks of a IIIV TFET technology platform against the 10-nm CMOS technology node considering 28T Full-Adders <b>2016</b> ,		1
13	Design guidelines for a metallization scheme with multiple-emitter contact lines in BC-BJ solar cells. <i>Journal of Computational Electronics</i> , <b>2016</b> , 15, 1498-1504	1.8	1

12	An Energy Aware Variation-Tolerant Writing Termination Control for STT-based Non Volatile Flip-Flops <b>2019</b> ,		1
11	Assessment of 2D-FET Based Digital and Analog Circuits on Paper. <i>Solid-State Electronics</i> , <b>2021</b> , 185, 108063	1.7	1
10	Assessment of paper-based MoS2 FET for Physically Unclonable Functions. <i>Solid-State Electronics</i> , <b>2022</b> , 194, 108391	1.7	1
9	Double-precision Dual Mode Logic carry-save multiplier. <i>The Integration VLSI Journal</i> , <b>2019</b> , 64, 71-77	1.4	0
8	Field-Free Magnetic Tunnel Junction for Logic Operations Based on Voltage-Controlled Magnetic Anisotropy. <i>IEEE Magnetism Letters</i> , <b>2021</b> , 12, 1-4	1.6	0
7	A 0.6V $\times$ 0.8V Compact Temperature Sensor with 0.24 $^{\circ}$ C Resolution, $\pm$ 1.4 $^{\circ}$ C Inaccuracy and 1.06 nJ per Conversion. <i>IEEE Sensors Journal</i> , <b>2022</b> , 1-1	4	0
6	Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. <i>Lecture Notes in Computer Science</i> , <b>2009</b> , 297-306	0.9	
5	An MTJ-Based Asynchronous System With Extremely Fine-Grained Voltage Scaling. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2021</b> , 68, 311-321	3.9	
4	Quantum capacitance transient phenomena in high-k dielectric armchair graphene nanoribbon field-effect transistor model. <i>Solid-State Electronics</i> , <b>2021</b> , 184, 108060	1.7	
3	Emerging Memory Structures for VLSI Circuits1-28		
2	Adjusting thermal stability in double-barrier MTJ for energy improvement in cryogenic STT-MRAMs. <i>Solid-State Electronics</i> , <b>2022</b> , 194, 108315	1.7	
1	Smart Material Implication Using Spin-Transfer Torque Magnetic Tunnel Junctions for Logic-in-Memory Computing. <i>Solid-State Electronics</i> , <b>2022</b> , 108390	1.7	