Marco Lanuzza

List of Publications by Year
in descending order

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128	1,759	304368	360668
papers	citations	22 h-index	35 g-index

130	130	130	1030
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Skyrmion based microwave detectors and harvesting. Applied Physics Letters, 2015, 107, .	1.5	86
2	Low-Power Level Shifter for Multi-Supply Voltage Designs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 922-926.	2.2	84
3	Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 388-391.	2.1	79
4	An Ultralow-Voltage Energy-Efficient Level Shifter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 61-65.	2.2	67
5	Digital and analog TFET circuits: Design and benchmark. Solid-State Electronics, 2018, 146, 50-65.	0.8	60
6	Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain. IEEE Transactions on Electron Devices, 2015, 62, 3973-3979.	1.6	59
7	Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits. IEEE Transactions on Electron Devices, 2017, 64, 2736-2743.	1.6	57
8	Gateâ€level body biasing technique for highâ€speed subâ€threshold CMOS logic gates. International Journal of Circuit Theory and Applications, 2014, 42, 65-70.	1.3	44
9	Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. IEEE Transactions on Electron Devices, 2016, 63, 2749-2756.	1.6	44
10	A Variation-Aware Timing Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1086-1095.	3.5	41
11	A Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs. IEEE Transactions on Electron Devices, 2017, 64, 4346-4353.	1.6	40
12	A high-performance fully reconfigurable FPGA-based 2D convolution processor. Microprocessors and Microsystems, 2005, 29, 381-391.	1.8	38
13	Low voltage logic circuits exploiting gate level dynamic body biasing in 28 nm UTBB FD-SOI. Solid-State Electronics, 2016, 117, 185-192.	0.8	38
14	Spinâ€“orbit torque based physical unclonable function. Journal of Applied Physics, 2020, 128, .	1.1	35
15	Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. Progress in Photovoltaics: Research and Applications, 2017, 25, 452-469.	4.4	33
16	An 88-fJ/40-MHz [0.4 V]â€“0.61-pJ/1-GHz [0.9 V] Dual-Mode Logic 8 <inline-formula> <tex-math notation="LaTeX">$imes$ </tex-math> </inline-formula> 8 bit Multiplier Accumulator With a Self-Adjustment Mechanism in 28-nm FD-SOI. IEEE Journal of Solid-State Circuits, 2019, 54, 560-568.	3.5	31
17	Comparative analysis of yield optimized pulsed flip-flops. Microelectronics Reliability, 2012, 52, 1679-1689.	0.9	28
18	Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework. IEEE Nanotechnology Magazine, 2017, 16, 160-168.	1.1	28

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19	Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. IEEE Journal of Solid-State Circuits, 2021, 56, 3134-3144.	3.5	27
20	Low-power split-path data-driven dynamic logic. IET Circuits, Devices and Systems, 2009, 3, 303-312.	0.9	26
21	Compact Modeling of Perpendicular STT-MTJs With Double Reference Layers. IEEE Nanotechnology Magazine, 2019, 18, 1063-1070.	1.1	25
22	Low bit rate image compression core for onboard space applications. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 114-128.	5.6	24
23	A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications. , 2007, , .		24
24	Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. Microelectronic Engineering, 2019, 215, 111009.	1.1	24
25	Designing High-Speed Adders in Power-Constrained Environments. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 172-176.	2.2	23
26	Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework. The Integration VLSI Journal, 2020, 71, 56-69.	1.3	22
27	Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications. IEEE Nanotechnology Magazine, 2021, 20, 123-128.	1.1	21
28	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications. , 2005, , .		19
29	Over/Undershooting Effects in Accurate Buffer Delay Model for Sub-Threshold Domain. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1456-1464.	3.5	18
30	Energyâ€efficient singleâ€clockâ€cycle binary comparator. International Journal of Circuit Theory and Applications, 2012, 40, 237-246.	1.3	17
31	Benchmarks of a III-V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits. Solid-State Electronics, 2017, 128, 37-42.	0.8	17
32	A 0.8-V, 1.54-pJ/940-MHz Dual-Mode Logic-Based 16Ã—16-b Booth Multiplier in 16-nm FinFET. IEEE Solid-State Circuits Letters, 2020, 3, 314-317.	1.3	17
33	A new low-power high-speed single-clock-cycle binary comparator. , 2010, , .		16
34	Impact of Process Variations on Flip-Flops Energy and Timing Characteristics. , 2010, , .		16
35	A physical unclonable function based on a 2â€transistor subthreshold voltage divider. International Journal of Circuit Theory and Applications, 2017, 45, 260-273.	1.3	16
36	A portable class of 3â€transistor current references with lowâ€power subâ€0.5Â<scp>V</scp> operation. International Journal of Circuit Theory and Applications, 2018, 46, 779-795.	1.3	16

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37	Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures. IEEE Transactions on Magnetics, 2021, 57, 1-6.	1.2	16
38	Gain-Cell Embedded DRAM Under Cryogenic Operationâ€"A First Study. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1319-1324.	2.1	16
39	Hamming Distance Tolerant Content-Addressable Memory (HD-CAM) for DNA Classification. IEEE Access, 2022, 10, 28080-28093.	2.6	16
40	Ultralow Voltage FinFET- Versus TFET-Based STT-MRAM Cells for IoT Applications. Electronics (Switzerland), 2021, 10, 1756.	1.8	14
41	Exploiting Self-Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications. ACM Transactions on Reconfigurable Technology and Systems, 2010, 4, 1-22.	1.9	13
42	A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1393-1397.	2.2	13
43	EDAM. , 2022, , .		13
44	Variable precision arithmetic circuits for FPGA-based multimedia processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 995-999.	2.1	12
45	A novel ICA-based hardware system for reconfigurable and portable BCI. , 2009, , .		12
46	Optimization of Rear Point Contact Geometry by Means of 3-D Numerical Simulation. Energy Procedia, 2012, 27, 197-202.	1.8	12
47	A 0.05 mmÂ², 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 749-753.	2.2	12
48	Relaxing non-volatility for energy-efficient DMTJ based cryogenic STT-MRAM. Solid-State Electronics, 2021, 184, 108090.	0.8	12
49	A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs. , 2010, , .		11
50	Evaluation of Dual Mode Logic in 28nm FD-SOI technology. , 2017, , .		11
51	A 0.6-to-1.8V CMOS Current Reference With Near-100% Power Utilization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3038-3042.	2.2	11
52	Static CMOS Physically Unclonable Function Based on 4T Voltage Divider With 0.6%â€"1.5% Bit Instability at 0.4â€"1.8 V Operation in 180 nm. IEEE Journal of Solid-State Circuits, 2022, 57, 2509-2520.	3.5	11
53	Embedded Memories for Cryogenic Applications. Electronics (Switzerland), 2022, 11, 61.	1.8	11
54	Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath. , 2009, , .		10

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55	Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis. Lecture Notes in Computer Science, 2011, , 180-189.	1.0	10
56	Exploring back biasing opportunities in 28nm UTBB FD-SOI technology for subthreshold digital design. , 2014, , .		10
57	Dynamic gate-level body biasing for subthreshold digital design. , 2014, , .		10
58	Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1639-1643.	2.2	10
59	Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. Journal of Low Power Electronics, 2009, 5, 326-338.	0.6	10
60	AIDA: Associative In-Memory Deep Learning Accelerator. IEEE Micro, 2022, 42, 67-75.	1.8	10
61	New performance/power/area efficient, reliable full adder design. , 2009, , .		9
62	Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. Journal of Low Power Electronics and Applications, 2011, 1, 97-108.	1.3	9
63	STT-MTJ Based Smart Implication for Energy-Efficient Logic-in-Memory Computing. Solid-State Electronics, 2021, 184, 108065.	0.8	9
64	Ultra-Low-Voltage Self-Body Biasing Scheme and Its Application to Basic Arithmetic Circuits. VLSI Design, 2015, 2015, 1-10.	0.5	8
65	Gateâ€level body biasing for subthreshold logic circuits: analytical modeling and design guidelines. International Journal of Circuit Theory and Applications, 2015, 43, 1523-1540.	1.3	8
66	An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. Lecture Notes in Computer Science, 2009, , 74-84.	1.0	7
67	Design of highâ€speed lowâ€power parallelâ€prefix adder trees in nanometer technologies. International Journal of Circuit Theory and Applications, 2014, 42, 731-743.	1.3	7
68	Extended exploration of low granularity back biasing control in 28nm UTBB FD-SOI technology. , 2016, , .		7
69	Design Space Exploration of Split-Path Data Driven Dynamic Full Adder. Journal of Low Power Electronics, 2010, 6, 469-481.	0.6	7
70	Analyzing noise robustness of wide fanâ€in dynamic logic gates under process variations. International Journal of Circuit Theory and Applications, 2014, 42, 452-467.	1.3	6
71	Impact of voltage scaling on STT-MRAMs through a variability-aware simulation framework. , 2017, , .		6
72	Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs. , 2019, , .		6

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73	A Low-Voltage, Low-Power Reconfigurable Current-Mode Softmax Circuit for Analog Neural Networks. Electronics (Switzerland), 2021, 10, 1004.	1.8	6
74	Exploiting Silicon Fingerprint for Device Authentication Using CMOS-PUF and ECC. , 2021, , .		5
75	Cost-effective low-power processor-in-memory-based reconfigurable datapath for multimedia applications. , 2005, , .		5
76	An efficient wavelet image encoder for FPGA-based designs. , 0, , .		4
77	Double-precision Dual Mode Logic carry-save multiplier. The Integration VLSI Journal, 2019, 64, 71-77.	1.3	4
78	Impact of Scaling on Physical Unclonable Function Based on Spinâ€“Orbit Torque. IEEE Magnetics Letters, 2020, 11, 1-5.	0.6	4
79	A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops. Journal of Low Power Electronics, 2013, 9, 445-451.	0.6	4
80	Field-Free Magnetic Tunnel Junction for Logic Operations Based on Voltage-Controlled Magnetic Anisotropy. IEEE Magnetics Letters, 2021, 12, 1-4.	0.6	4
81	Making IoT Services Accountable: A Solution Based on Blockchain and Physically Unclonable Functions. Lecture Notes in Computer Science, 2019, , 294-305.	1.0	4
82	A 0.6Vâ€“1.8V Compact Temperature Sensor With 0.24 Â°C Resolution, Â±1.4 Â°C Inaccuracy and 1.06nJ per Conversion. IEEE Sensors Journal, 2022, 22, 11480-11488.	2.4	4
83	Assessment of paper-based MoS2 FET for Physically Unclonable Functions. Solid-State Electronics, 2022, 194, 108391.	0.8	4
84	Performance and reliability of ultra-thin oxide nMOSFETs under variable body bias. Microelectronic Engineering, 2007, 84, 1947-1950.	1.1	3
85	Understanding the impact of point-contact scheme and selective emitter in a c-Si BC-BJ solar cell by full 3D numerical simulations. Solar Energy, 2017, 155, 1443-1450.	2.9	3
86	Design of a sub-1-V nanopower CMOS current reference. , 2017, , .		3
87	Low energy/delay overhead level shifter for wideâ€range voltage conversion. International Journal of Circuit Theory and Applications, 2017, 45, 1637-1646.	1.3	3
88	Simulations and comparisons of basic analog and digital circuit blocks employing Tunnel FETs and conventional FinFETs. , 2017, , .		3
89	A variation-aware simulation framework for hybrid CMOS/spintronic circuits. , 2017, , .		3
90	Live Demo: An 88fJ / 40 MHz [0.4V] â€“ 0.61pJ / 1GHz [0.9V] Dual Mode Logic 8Ã—8-Bit Multiplier Accumulator with a Self-Adjustment Mechanism in 28 nm FD-SOI. , 2019, , .		3

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91	Robust Dual Mode Pass Logic (DMPL) for Energy Efficiency and High Performance. , 2020, , .		3
92	Assessment of 2D-FET Based Digital and Analog Circuits on Paper. Solid-State Electronics, 2021, 185, 108063.	0.8	3
93	A 3.2-pW, 0.2-V Trimming-Less Voltage Reference with 1.4-mV Across-Wafer Total Accuracy. , 2021, , .		3
94	Low-cost fully reconfigurable data-path for FPGA-based multimedia processor. , 0, , .		2
95	Design and evaluation of high-speed energy-aware carry skip adders. , 2010, , .		2
96	A Comparative Study of MWT Architectures by Means of Numerical Simulations. Energy Procedia, 2013, 38, 131-136.	1.8	2
97	Improving speed and power characteristics of pulse-triggered flip-flops. , 2014, , .		2
98	Low voltage ripple carry adder with low-granularity dynamic forward back-biasing in 28 nm UTBB FD-SOI. , 2015, , .		2
99	Design guidelines for a metallization scheme with multiple-emitter contact lines in BC-BJ solar cells. Journal of Computational Electronics, 2016, 15, 1498-1504.	1.3	2
100	An Energy Aware Variation-Tolerant Writing Termination Control for STT-based Non Volatile Flip-Flops. , 2019, , .		2
101	A 0.25-V, 5.3-pW Voltage Reference with 25-Î¼V/Â°C Temperature Coefficient, 140-Î¼V/V Line Sensitivity and 2,200-Î¼m² Area in 180nm. , 2020, , .		2
102	A New Optimized High-Speed Low-Power Data-Driven Dynamic (D3L) 32-Bit Kogge-Stone Adder. Lecture Notes in Computer Science, 2010, , 357-366.	1.0	2
103	Adjusting thermal stability in double-barrier MTJ for energy improvement in cryogenic STT-MRAMs. Solid-State Electronics, 2022, 194, 108315.	0.8	2
104	Smart Material Implication Using Spin-Transfer Torque Magnetic Tunnel Junctions for Logic-in-Memory Computing. Solid-State Electronics, 2022, 194, 108390.	0.8	2
105	Designing Dynamic Carry Skip Adders: Analysis and Comparison. Circuits, Systems, and Signal Processing, 2014, 33, 1019-1034.	1.2	1
106	Benchmarks of a IIIâ€“V TFET technology platform against the 10-nm CMOS technology node considering 28T Full-Adders. , 2016, , .		1
107	Early assessment of tunnel-FET for energy-efficient logic circuits. , 2016, , .		1
108	Energy-delay tradeoffs of low-voltage dual mode logic in 28nm FD-SOI. , 2017, , .		1

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109	Device-to-System Level Simulation Framework for STT-DMTJ Based Cache Memory. , 2019, , .		1
110	High-Speed and Low-Energy Dual-Mode Logic based Single-Clack-Cycle Binary Comparator. , 2021, , .		1
111	Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. Lecture Notes in Computer Science, 2009, , 297-306.	1.0	1
112	Design of Ultra-Low Voltage/Power Circuits and Systems. Electronics (Switzerland), 2022, 11, 607.	1.8	1
113	Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories. , 2022, , .		1
114	Design and Implementation of a 90nm Low bit-rate Image Compression Core. , 2007, , .		0
115	Impact of Random Process Variations on Different 65nm SRAM Cell Topologies. , 2010, , .		0
116	Self-repairing SRAM architecture to mitigate the inter-die process variations at 65nm technology. Proceedings of SPIE, 2011, , .	0.8	0
117	Hardware implementation of a Test Lab for Smart Home environments. , 2015, , .		0
118	A virtual III-V tunnel FET technology platform for ultra-low voltage comparators and level shifters. , 2017, , .		0
119	Impact of the Emitter Contact Pattern in c-Si BC- BJ Solar Cells by Numerical Simulations. , 2018, , .		0
120	Design of a 3T current reference for low-voltage, low-power operation. , 2018, , .		0
121	Evaluating the Energy Efficiency of STT-MRAMs Based on Perpendicular MTJs with Double Reference Layers. , 2019, , .		0
122	Exploiting Single-Well Design for Energy-Efficient Ultra-Wide Voltage Range Dual Mode Logic-Based Digital Circuits in 28nm FD-SOI Technology. , 2020, , .		0
123	An MTJ-Based Asynchronous System With Extremely Fine-Grained Voltage Scaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 311-321.	3.5	0
124	RF-DC Multiplier for RF Energy Harvester based on 32nm and TFET technologies. , 2021, , .		0
125	Live Demonstration: A 0.8V, 1.54 pJ / 940 MHz Dual Mode Logic-Based 16x16-Bit Booth Multiplier in 16-nm FinFET. , 2021, , .		0
126	Live Demo: Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths. , 2021, , .		0

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127	Quantum capacitance transient phenomena in high-k dielectric armchair graphene nanoribbon field-effect transistor model. Solid-State Electronics, 2021, 184, 108060.	0.8	0
128	A 180 nm Low-Cost Operational Amplifier for IoT Applications. , 2021, , .		0