Chun Jason Xue

List of Publications by Year
in descending order

192	2,473	361045	476904
papers	citations	20 h-index	29 g-index

192	192	192	1176
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Emerging non-volatile memories. , 2011, , .		165
2	Reducing write activities on non-volatile memories in embedded CMPs via data migration and recomputation. , 2010, , .		96
3	Dynamic Localisation of Mature MicroRNAs in Human Nucleoli is Influenced by Exogenous Genetic Materials. PLoS ONE, 2013, 8, e70869.	1.1	71
4	STT-RAM based energy-efficiency hybrid cache for CMPs. , 2011, , .		63
5	Loop scheduling and bank type assignment for heterogeneous multi-bank memory. Journal of Parallel and Distributed Computing, 2009, 69, 546-558.	2.7	60
6	Exploiting parallelism in I/O scheduling for access conflict minimization in flash-based solid state drives. , 2014, , .		60
7	Data Allocation Optimization for Hybrid Scratch Pad Memory With SRAM and Nonvolatile Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1094-1102.	2.1	54
8	Write activity reduction on flash main memory via smart victim cache. , 2010, , .		48
9	Quality-retaining OLED dynamic voltage scaling for video streaming applications on mobile devices. , 2012, , .		48
10	Software Enabled Wear-Leveling for Hybrid PCM Main Memory on Embedded Systems. , 2013, , .		46
11	Minimizing WCET for Real-Time Embedded Systems via Static Instruction Cache Locking. , 2009, , .		45
12	SLC-enabled Wear Leveling for MLC PCM Considering Process Variation. , 2014, , .		44
13	Write Activity Minimization for Nonvolatile Main Memory Via Scheduling and Recomputation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 584-592.	1.9	42
14	Write activity reduction on non-volatile main memories for embedded chip multiprocessors. Transactions on Embedded Computing Systems, 2013, 12, 1-27.	2.1	42
15	ExLRU. , 2011, , .		37
16	Exploiting Process Variation for Write Performance Improvement on NAND Flash Memory Storage Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 334-337.	2.1	33
17	Improving LDPC performance via asymmetric sensing level placement on flash memory. , 2017, , .		33
18	Data Rate Fingerprinting: A WLAN-Based Indoor Positioning Technique for Passive Localization. IEEE Sensors Journal, 2019, 19, 6517-6529.	2.4	33

#	Article	IF	Citations
19	MAC. , 2012, , .		32
20	Compiler-Assisted STT-RAM-Based Hybrid Cache for Energy Efficient Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1829-1840.	2.1	32
21	Retention Trimming for Lifetime Improvement of Flash Memory Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 58-71.	1.9	32
22	Exploiting Parallelism for Access Conflict Minimization in Flash-Based Solid State Drives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 168-181.	1.9	32
23	Towards energy efficient hybrid on-chip Scratch Pad Memory with non-volatile memory. , 2011, , .		28
24	Low Overhead Software Wear Leveling for Hybrid PCM + DRAM Main Memory on Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 654-663.	2.1	28
25	Solar Power Prediction Assisted Intra-task Scheduling for Nonvolatile Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 724-737.	1.9	26
26	Reducing LDPC Soft Sensing Latency by Lightweight Data Refresh for Flash Read Performance Improvement. , 2017, , .		26
27	Task Assignment with Cache Partitioning and Locking for WCET Minimization on MPSoC. , 2010, , .		25
28	Minimizing Access Cost for Multiple Types of Memory Units in Embedded Systems Through Data Allocation and Scheduling. IEEE Transactions on Signal Processing, 2012, 60, 3253-3263.	3.2	25
29	Stack-Size Sensitive On-Chip Memory Backup for Self-Powered Nonvolatile Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1804-1816.	1.9	24
30	ApproxFTL: On the Performance and Lifetime Improvement of 3-D NAND Flash-Based SSDs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1957-1970.	1.9	24
31	Exploiting set-level write non-uniformity for energy-efficient NVM-based hybrid cache. , 2011, , .		23
32	Instruction cache locking for multi-task real-time embedded systems. Real-Time Systems, 2012, 48, 166-197.	1.1	22
33	Minimizing MLC PCM write energy for free through profiling-based state remapping. , 2015, , .		22
34	Efficient Data Placement for Improving Data Access Performance on Domain-Wall Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3094-3104.	2.1	22
35	Reprogramming with Minimal Transferred Data on Wireless Sensor Network. , 2009, , .		21
36	Management and optimization for nonvolatile memory-based hybrid scratchpad memory on multicore embedded processors. Transactions on Embedded Computing Systems, 2014, 13, 1-25.	2.1	21

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37	Task Allocation on Nonvolatile-Memory-Based Hybrid Main Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1271-1284.	2.1	20
38	Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache. IEEE Transactions on Computers, 2015, 64, 2169-2181.	2.4	20
39	Data Backup Optimization for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1660-1673.	1.9	20
40	Minimizing Retention Induced Refresh Through Exploiting Process Variation of Flash Memory. IEEE Transactions on Computers, 2019, 68, 83-98.	2.4	20
41	Software Assisted Non-volatile Register Reduction for Energy Harvesting Based Cyber-Physical System. , 2015, , .		19
42	Hybrid nonvolatile disk cache for energy-efficient and high-performance systems. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-23.	1.9	18
43	Leveling to the last mile: Near-zero-cost bit level wear leveling for PCM-based main memory. , 2014, , .		18
44	Exploiting Process Variation for Retention Induced Refresh Minimization on Flash Memory. , 2016, , .		18
45	Iterational retiming with partitioning. Transactions on Embedded Computing Systems, 2010, 9, 1-26.	2.1	16
46	Cooperating Write Buffer Cache and Virtual Memory Management for Flash Memory Based Systems. , 2011, , .		16
47	Wear-Leveling Aware Page Management for Non-Volatile Main Memory on Embedded Systems. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 129-142.	2.5	16
48	EMC: Energy-Aware Morphable Cache Design for Non-Volatile Processors. IEEE Transactions on Computers, 2019, 68, 498-509.	2.4	16
49	Minimizing write activities to non-volatile memory via scheduling and recomputation. , 2010, , .		15
50	Compiler-assisted preferred caching for embedded systems with STT-RAM based hybrid cache. , 2012, , .		15
51	Instruction Cache Locking for Embedded Systems using Probability Profile. Journal of Signal Processing Systems, 2012, 69, 173-188.	1.4	15
52	Low-energy volatile STT-RAM cache design using cache-coherence-enabled adaptive refresh. ACM Transactions on Design Automation of Electronic Systems, 2013, 19, 1-23.	1.9	15
53	Joint task assignment and cache partitioning with cache locking for WCET minimization on MPSoC. Journal of Parallel and Distributed Computing, 2011, 71, 1473-1483.	2.7	14
54	Error Model Guided Joint Performance and Endurance Optimization for Flash Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 343-355.	1.9	14

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55	Wear Relief for High-Density Phase Change Memory Through Cell Morphing Considering Process Variation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 227-237.	1.9	14
56	Exploiting Chip Idleness for Minimizing Garbage Collectionâ€"Induced Chip Access Conflict on SSDs. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-29.	1.9	14
57	A Wear Leveling Aware Memory Allocator for Both Stack and Heap Management in PCM-based Main Memory Systems. , 2019, , .		14
58	MGC: Multiple graph-coloring for non-volatile memory based hybrid Scratchpad Memory. , 2012, , .		13
59	Training neural-network-based controller on distributed machine learning platform for power electronics systems. , 2017, , .		13
60	Shadow Block: Accelerating ORAM Accesses with Data Duplication. , 2018, , .		13
61	Combining Coarse-Grained Software Pipelining with DVS for Scheduling Real-Time Periodic Dependent Tasks on Multi-Core Embedded Systems. Journal of Signal Processing Systems, 2009, 57, 249-262.	1.4	12
62	Register allocation for write activity minimization on non-volatile main memory. , 2011, , .		12
63	Cooperating Virtual Memory and Write Buffer Management for Flash-Based Storage Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 706-719.	2.1	12
64	State Asymmetry Driven State Remapping in Phase Change Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 27-40.	1.9	12
65	Access Characteristic Guided Read and Write Regulation on Flash Based Storage Systems. IEEE Transactions on Computers, 2018, 67, 1663-1676.	2.4	12
66	Boosting the Performance of SSDs via Fully Exploiting the Plane Level Parallelism. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 2185-2200.	4.0	12
67	Maximizing IO Performance Via Conflict Reduction for Flash Memory Storage Systems. , 2015, , .		12
68	Migration-Aware Loop Retiming for STT-RAM-Based Hybrid Cache in Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 329-342.	1.9	11
69	Checkpointing-Aware Loop Tiling for Energy Harvesting Powered Nonvolatile Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 15-28.	1.9	11
70	Process Variation Aware Read Performance Improvement for LDPC-Based nand Flash Memory. IEEE Transactions on Reliability, 2020, 69, 310-321.	3.5	11
71	Acceleration of Composite Order Bilinear Pairing on Graphics Hardware. Lecture Notes in Computer Science, 2012, , 341-348.	1.0	11
72	Optimizing Data Allocation and Memory Configuration for Non-Volatile Memory Based Hybrid SPM on Embedded CMPs. , 2012, , .		10

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73	Power-Aware Variable Partitioning for DSPs With Hybrid PRAM and DRAM Main Memory. IEEE Transactions on Signal Processing, 2013, 61, 3509-3520.	3.2	10
74	Exploit asymmetric error rates of cell states to improve the performance of flash memory storage systems. , 2014, , .		10
75	Sleep-aware variable partitioning for energy-efficient hybrid PRAM and DRAM main memory. , 2014, , .		10
76	A Unified Write Buffer Cache Management Scheme for Flash Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2779-2792.	2.1	10
77	Timing optimization via nest-loop pipelining considering code size. Microprocessors and Microsystems, 2008, 32, 351-363.	1.8	9
78	Optimized address assignment with array and loop transformations for minimizing schedule length. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 379-389.	3.5	9
79	Address assignment sensitive variable partitioning and scheduling for DSPS with multiple memory banks. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	9
80	NVM-Based FPGA Block RAM With Adaptive SLC-MLC Conversion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2661-2672.	1.9	9
81	File Fragmentation in Mobile Devices: Measurement, Evaluation, and Treatment. IEEE Transactions on Mobile Computing, 2019, 18, 2062-2076.	3.9	9
82	FPGA-based Compaction Engine for Accelerating LSM-tree Key-Value Stores. , 2020, , .		9
83	Instruction Cache Locking for Real-Time Embedded Systems with Multi-tasks. , 2009, , .		8
84	LADPM: Latency-Aware Dual-Partition Multicast Routing for Mesh-Based Network-on-Chips. , 2010, , .		8
85	Optimal task allocation on non-volatile memory based hybrid main memory. , 2011, , .		8
86	Register allocation for write activity minimization on non-volatile main memory for embedded systems. Journal of Systems Architecture, 2012, 58, 13-23.	2.5	8
87	Cache Coherence Enabled Adaptive Refresh for Volatile STT-RAM. , 2013, , .		8
88	Online OLED dynamic voltage scaling for video streaming applications on mobile devices. , 2013, , .		8
89	Register allocation for hybrid register architecture in nonvolatile processors. , 2014, , .		8
90	An I/O Scheduling Strategy for Embedded Flash Storage Devices With Mapping Cache. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 756-769.	1.9	8

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91	WCET-aware re-scheduling register allocation for real-time embedded systems with clustered VLIW architecture. , 2012, , .		7
92	Retention trimming for wear reduction of flash memory storage systems. , 2014, , .		7
93	Scheduling to Optimize Cache Utilization for Non-Volatile Main Memories. IEEE Transactions on Computers, 2014, 63, 2039-2051.	2.4	7
94	Maximizing Forward Progress with Cache-aware Backup for Self-powered Non-volatile Processors. , 2017, , .		7
95	An empirical study of F2FS on mobile devices. , 2017, , .		7
96	Energy, latency, and lifetime improvements in MLC NVM with enhanced WOM code. , 2018, , .		7
97	Optimizing Scheduling and Intercluster Connection for Application-Specific DSP Processors. IEEE Transactions on Signal Processing, 2009, 57, 4538-4547.	3.2	6
98	Analysis and approximation for bank selection instruction minimization on partitioned memory architecture. , 2010, , .		6
99	Sleep-aware mode assignment in wireless embedded systems. Journal of Parallel and Distributed Computing, 2011, 71, 1002-1010.	2.7	6
100	Branch Prediction-Directed Dynamic Instruction Cache Locking for Embedded Systems. Transactions on Embedded Computing Systems, 2014, 13, 1-24.	2.1	6
101	WCET-Aware Re-Scheduling Register Allocation for Real-Time Embedded Systems With Clustered VLIW Architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 168-180.	2.1	6
102	Dynamic merging/splitting for better responsiveness in mobile devices. , 2016, , .		6
103	Write Mode Aware Loop Tiling for High Performance Low Power Volatile PCM in Embedded Systems. IEEE Transactions on Computers, 2016, 65, 2313-2324.	2.4	6
104	Energy-aware morphable cache management for self-powered non-volatile processors. , 2017, , .		6
105	DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2981-2994.	2.1	6
106	Energy Optimal Task Scheduling with Normally-off Local Memory and Sleep-aware Shared Memory with Access Conflict. IEEE Transactions on Computers, 2018, , 1-1.	2.4	6
107	Real-Time Data Retrieval in Cyber-Physical Systems with Temporal Validity and Data Availability Constraints. IEEE Transactions on Knowledge and Data Engineering, 2019, 31, 1779-1793.	4.0	6
108	Compiler directed write-mode selection for high performance low power volatile PCM. ACM SIGPLAN Notices, 2013, 48, 101-110.	0.2	6

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109	RM-SSD: In-Storage Computing for Large-Scale Recommendation Inference. , 2022, , .		6
110	Real-Time Loop Scheduling with Leakage Energy Minimization for Embedded VLIW DSP Processors. Gifted and Talented International, 2007, , .	0.2	5
111	Optimal scheduling to minimize non-volatile memory access time with hardware cache. , 2010, , .		5
112	Code Motion for Migration Minimization in STT-RAM Based Hybrid Cache. , 2012, , .		5
113	Memory access schedule minimization for embedded systems. Journal of Systems Architecture, 2012, 58, 48-59.	2.5	5
114	Minimizing accumulative memory load cost on multi-core DSPs with multi-level memory. Journal of Systems Architecture, 2013, 59, 389-399.	2.5	5
115	Write Mode Aware Loop Tiling for High Performance Low Power Volatile PCM. , 2014, , .		5
116	A wear-leveling-aware dynamic stack for PCM memory in embedded systems. , 2014, , .		5
117	Maximizing Common Idle Time on Multi-Core Processors with Shared Memory. , 2015, , .		5
118	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2153-2163.	2.1	5
119	Race to idle or not: balancing the memory sleep time with DVS for energy minimization. Journal of Combinatorial Optimization, 2018, 35, 860-894.	0.8	5
120	Real-Time Data Retrieval With Multiple Availability Intervals in CPS Under Freshness Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2743-2754.	1.9	5
121	Reinforcement Learning based Background Segment Cleaning for Log-structured File System on Mobile Devices. , 2019, , .		5
122	1+1>2: variation-aware lifetime enhancement for embedded 3D NAND flash systems. , 2019, , .		5
123	Applying Multiple Level Cell to Non-volatile FPGAs. Transactions on Embedded Computing Systems, 2020, 19, 1-22.	2.1	5
124	Energy-Efficient Joint Scheduling and Application-Specific Interconnection Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1813-1822.	2.1	4
125	Loop fusion and reordering for register file optimization on stream processors. Journal of Systems and Software, 2012, 85, 1673-1681.	3.3	4
126	Migration-aware loop retiming for STT-RAM based hybrid cache for embedded systems. , 2013, , .		4

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127	Register allocation for embedded systems to simultaneously reduce energy and temperature on registers. Transactions on Embedded Computing Systems, 2013, 13, 1-26.	2.1	4
128	Retention Trimming for Wear Reduction of Flash Memory Storage Systems. , 2014, , .		4
129	Improving MLC PCM write throughput by write reconstruction. , 2015, , .		4
130	Maximizing Common Idle Time on Multicore Processors With Shared Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2095-2108.	2.1	4
131	Energy Efficient Operating Mode Assignment for Real-Time Tasks in Wireless Embedded Systems. , 2008, , .		3
132	Variable Length Pattern Matching for Hardware Network Intrusion Detection System. Journal of Signal Processing Systems, 2010, 59, 85-93.	1.4	3
133	Minimizing Schedule Length via Cooperative Register Allocation and Loop Scheduling for Embedded Systems. , 2011, , .		3
134	Compiler directed write-mode selection for high performance low power volatile PCM. , 2013, , .		3
135	Thread Progress Aware Coherence Adaption for Hybrid Cache Coherence Protocols. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 2697-2707.	4.0	3
136	Non-volatile registers aware instruction selection for embedded systems. , 2014, , .		3
137	Joint Profit and Process Variation Aware High Level Synthesis With Speed Binning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1640-1650.	2.1	3
138	Joint WCET and Update Activity Minimization for Cyber-Physical Systems. Transactions on Embedded Computing Systems, 2015, 14, 1-21.	2.1	3
139	Minimizing cell-to-cell interference by exploiting differential bit impact characteristics of scaled MLC NAND flash memories. , 2016, , .		3
140	Peak-to-average pumping efficiency improvement for charge pump in Phase Change Memories. , 2016, , .		3
141	Thread Criticality Assisted Replication and Migration for Chip Multiprocessor Caches. IEEE Transactions on Computers, 2017, 66, 1747-1762.	2.4	3
142	Runtime and reconfiguration dual-aware placement for SRAM-NVM hybrid FPGAs. , 2017, , .		3
143	Selective Compression Scheme for Read Performance Improvement on Flash Devices. , 2018, , .		3
144	Work-in-Progress: Revisiting Wear Leveling Design on Compression Applied 3D NAND Flash Memory. , 2018, , .		3

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145	Accelerating Monte Carlo Bayesian Prediction via Approximating Predictive Uncertainty Over the Simplex. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 1492-1506.	7.2	3
146	Effective Loop Partitioning and Scheduling under Memory and Register Dual Constraints. , 2008, , .		2
147	Energy-aware register file re-partitioning for clustered VLIW architectures. , 2009, , .		2
148	Minimizing Memory Access Schedule for Memories. , 2009, , .		2
149	Co-optimization of memory access and task scheduling on MPSoC architectures with multi-level memory. , 2010, , .		2
150	TEACA: Thread ProgrEss Aware Coherence Adaption for hybrid coherence protocols. , 2012, , .		2
151	Dual partitioning multicasting for high-performance on-chip networks. Journal of Parallel and Distributed Computing, 2014, 74, 1858-1871.	2.7	2
152	C3: Cooperative Code Positioning and Cache Locking for WCET Minimization. , 2015, , .		2
153	Improving read performance via selective V_{pass} reduction on high density 3D NAND flash memory. , 2017, , .		2
154	Enhancing SSD performance with LDPC-aware garbage collection. , 2017, , .		2
155	Fair Down to the Device: A GC-Aware Fair Scheduler for SSD. , 2019, , .		2
156	Online Rare Category Detection for Edge Computing. , 2019, , .		2
157	Read-Ahead Efficiency on Mobile Devices: Observation, Characterization, and Optimization. IEEE Transactions on Computers, 2021, 70, 99-110.	2.4	2
158	iTRIM: I/O-Aware TRIM for Improving User Experience on Mobile Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1782-1795.	1.9	2
159	Tail Latency Optimization for LDPC-Based High-Density and Low-Cost Flash Memory Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 544-557.	1.9	2
160	Race to Idle or Not : Balancing the Memory Sleep Time with DVS for Energy Minimization. , 2015, , .		2
161	A Formal Specification and Verification Framework for Designing and Verifying Reliable and Dependable Software for Computerized Numerical Control (CNC) Systems. , 2008, , .		1
162	Joint variable partitioning and bank selection instruction optimization on embedded systems with multiple memory banks. , 2010, , .		1

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163	Register allocation for simultaneous reduction of energy and peak temperature on registers. , 2011, , .		1
164	Poster Abstract: Smart Phone Lift for Improving Energy Efficiency and User Comfort in Green Buildings. , 2012, , .		1
165	Analysis and approximation for bank selection instruction minimization on partitioned memory architecture. Journal of Combinatorial Optimization, 2012, 23, 274-291.	0.8	1
166	Branch Prediction directed Dynamic instruction Cache Locking for embedded systems. , 2013, , .		1
167	Minimizing code size via page selection optimization on partitioned memory architectures. , 2013, , .		1
168	Compiler-assisted refresh minimization for volatile STT-RAM cache. , 2013, , .		1
169	Data re-allocation enabled cache locking for embedded systems. , 2013, , .		1
170	A wear-leveling-aware dynamic stack for PCM memory in embedded systems. , 2014, , .		1
171	Minimizing Leakage Energy with Modulo Scheduling for VLIW DSP Processors. International Federation for Information Processing, 2008, , 111-120.	0.4	1
172	TRACE: A Fast Transformer-based General-Purpose Lossless Compressor. , 2022, , .		1
173	Read latency variation aware performance optimization on high-density NAND flash based storage systems. CCF Transactions on High Performance Computing, 2022, 4, 265-280.	1.1	1
174	Loop scheduling and assignment to minimize energy while hiding latency for heterogeneous multi-bank memory. , 2008, , .		0
175	Computation and data transfer co-scheduling for interconnection bus minimization. , 2009, , .		0
176	Analysis and approximation for bank selection instruction minimization on partitioned memory architecture. ACM SIGPLAN Notices, 2010, 45, 1-8.	0.2	0
177	Energy efficient joint scheduling and multi-core interconnect design. , 2010, , .		0
178	Fine-grained adaptive CMP cache sharing through access history exploitation. , 2010, , .		0
179	Migration-aware adaptive MPSoC static schedules with dynamic reconfigurability. Journal of Parallel and Distributed Computing, 2011, 71, 1400-1410.	2.7	0
180	Loop fusion and reordering for register file optimization on stream processors. , 2011, , .		0

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181	Guest Editorial Special Section on Memory Architectures and Organization. IEEE Embedded Systems Letters, 2012, 4, 81-81.	1.3	0
182	PRR: A low-overhead cache replacement algorithm for embedded processors. , 2012, , .		0
183	Algorithms to Minimize Data Transfer for Code Update on Wireless Sensor Network. Journal of Signal Processing Systems, 2013, 71, 143-157.	1.4	0
184	WUCC: Joint WCET and Update Conscious Compilation for cyber-physical systems. , 2013, , .		0
185	Joint variable partitioning and bank selection instruction optimization for partitioned memory architectures. Transactions on Embedded Computing Systems, 2013, 12, 1-27.	2.1	0
186	Near Data Filtering for Distributed Database Systems. , 2018, , .		0
187	NVLH: Crash-Consistent Linear Hashing for Non-Volatile Memory. , 2018, , .		0
188	Checkpointing-aware Data Allocation for Energy Harvesting Powered Non-volatile Processors. , 2019, , .		0
189	Online Rare Category Identification and Data Diversification for Edge Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1290-1301.	1.9	0
190	Single and Multiple Device DSA Problem, Complexities and Online Algorithms. Lecture Notes in Computer Science, 2010, , 218-229.	1.0	0
191	Optimize Address Assignment With Array and Loop Transformations for Minimizing Schedule Length. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2008, , .	0.1	0
192	NetKernel: Making Network Stack Part of the Virtualized Infrastructure. IEEE/ACM Transactions on Networking, 2022, 30, 999-1013.	2.6	0