Chun Jason Xue

List of Publications by Citations

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

166 papers	1,737 citations	20 h-index	32 g-index
192 ext. papers	2,130 ext. citations	2.4 avg, IF	4.76 L-index

#	Paper	IF	Citations
166	Emerging non-volatile memories **2011**,		121
165	Reducing write activities on non-volatile memories in embedded CMPs via data migration and recomputation **2010**,		79
164	STT-RAM based energy-efficiency hybrid cache for CMPs **2011**,		53
163	Dynamic localisation of mature microRNAs in Human nucleoli is influenced by exogenous genetic materials. *PLoS ONE*, **2013**, 8, e70869	3.7	45
162	Exploiting parallelism in I/O scheduling for access conflict minimization in flash-based solid state drives **2014**,		42
161	Data Allocation Optimization for Hybrid Scratch Pad Memory With SRAM and Nonvolatile Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1094-1102	2.6	41
160	Minimizing WCET for Real-Time Embedded Systems via Static Instruction Cache Locking **2009**,		41
159	Write activity reduction on flash main memory via smart victim cache **2010**,		41
158	Software Enabled Wear-Leveling for Hybrid PCM Main Memory on Embedded Systems **2013**,		37
157	Quality-retaining OLED dynamic voltage scaling for video streaming applications on mobile devices **2012**,		35
156	Write Activity Minimization for Nonvolatile Main Memory Via Scheduling and Recomputation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 584-592	2.5	34
155	SLC-enabled Wear Leveling for MLC PCM Considering Process Variation **2014**,		31
154	Compiler-Assisted STT-RAM-Based Hybrid Cache for Energy Efficient Embedded Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1829-1840	2.6	30
153	Write activity reduction on non-volatile main memories for embedded chip multiprocessors. *Transactions on Embedded Computing Systems*, **2013**, 12, 1-27	1.8	30
152	MAC **2012**,		28
151	ExLRU **2011**,		26
150	Solar Power Prediction Assisted Intra-task Scheduling for Nonvolatile Sensor Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 724-737	2.5	24

149	Task Assignment with Cache Partitioning and Locking for WCET Minimization on MPSoC **2010**,		23
148	Improving LDPC performance via asymmetric sensing level placement on flash memory **2017**,		21
147	Minimizing Access Cost for Multiple Types of Memory Units in Embedded Systems Through Data Allocation and Scheduling. *IEEE Transactions on Signal Processing*, **2012**, 60, 3253-3263	4.8	21
146	Retention Trimming for Lifetime Improvement of Flash Memory Storage Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 58-71	2.5	20
145	Exploiting Process Variation for Write Performance Improvement on NAND Flash Memory Storage Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 334-337	2.6	19
144	Instruction cache locking for multi-task real-time embedded systems. *Real-Time Systems*, **2012**, 48, 166-197	2.5	19
143	Low Overhead Software Wear Leveling for Hybrid PCM + DRAM Main Memory on Embedded Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 654-663	2.6	18
142	Exploiting Parallelism for Access Conflict Minimization in Flash-Based Solid State Drives. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 168-181	2.5	18
141	Task Allocation on Nonvolatile-Memory-Based Hybrid Main Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1271-1284	2.6	17
140	Management and optimization for nonvolatile memory-based hybrid scratchpad memory on multicore embedded processors. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-25	1.8	17
139	Stack-Size Sensitive On-Chip Memory Backup for Self-Powered Nonvolatile Processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1804-1816	2.5	16
138	ApproxFTL: On the Performance and Lifetime Improvement of 3-D NAND Flash-Based SSDs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1957-1970	2.5	16
137	Exploiting set-level write non-uniformity for energy-efficient NVM-based hybrid cache **2011**,		16
136	Software assisted non-volatile register reduction for energy harvesting based cyber-physical system **2015**,		16
135	Data Backup Optimization for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 1660-1673	2.5	15
134	Data Rate Fingerprinting: A WLAN-Based Indoor Positioning Technique for Passive Localization. *IEEE Sensors Journal*, **2019**, 19, 6517-6529	4	15
133	Minimizing MLC PCM write energy for free through profiling-based state remapping **2015**,		15
132	Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache. *IEEE Transactions on Computers*, **2015**, 64, 2169-2181	2.5	15

131	Cooperating Write Buffer Cache and Virtual Memory Management for Flash Memory Based Systems **2011**,		15
130	Loop scheduling and bank type assignment for heterogeneous multi-bank memory. *Journal of Parallel and Distributed Computing*, **2009**, 69, 546-558	4.4	15
129	Wear Relief for High-Density Phase Change Memory Through Cell Morphing Considering Process Variation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 227-237	2.5	14
128	Joint task assignment and cache partitioning with cache locking for WCET minimization on MPSoC. *Journal of Parallel and Distributed Computing*, **2011**, 71, 1473-1483	4.4	14
127	Iterational retiming with partitioning. *Transactions on Embedded Computing Systems*, **2010**, 9, 1-26	1.8	14
126	Reprogramming with Minimal Transferred Data on Wireless Sensor Network **2009**,		14
125	Wear-Leveling Aware Page Management for Non-Volatile Main Memory on Embedded Systems. *IEEE Transactions on Multi-Scale Computing Systems*, **2016**, 2, 129-142		13
124	Reducing LDPC Soft Sensing Latency by Lightweight Data Refresh for Flash Read Performance Improvement **2017**,		13
123	Instruction Cache Locking for Embedded Systems using Probability Profile. *Journal of Signal Processing Systems*, **2012**, 69, 173-188	1.4	13
122	Low-energy volatile STT-RAM cache design using cache-coherence-enabled adaptive refresh. *ACM Transactions on Design Automation of Electronic Systems*, **2013**, 19, 1-23	1.5	13
121	Compiler-assisted preferred caching for embedded systems with STT-RAM based hybrid cache **2012** ,		13
120	Minimizing Retention Induced Refresh Through Exploiting Process Variation of Flash Memory. *IEEE Transactions on Computers*, **2019**, 68, 83-98	2.5	12
119	Error Model Guided Joint Performance and Endurance Optimization for Flash Memory. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 343-355	2.5	12
118	Leveling to the last mile: Near-zero-cost bit level wear leveling for PCM-based main memory **2014**,		12
117	Cooperating Virtual Memory and Write Buffer Management for Flash-Based Storage Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 706-719	2.6	12
116	Efficient Data Placement for Improving Data Access Performance on Domain-Wall Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 3094-3104	2.6	12
115	Hybrid nonvolatile disk cache for energy-efficient and high-performance systems. *ACM Transactions on Design Automation of Electronic Systems*, **2013**, 18, 1-23	1.5	11
114	Register allocation for write activity minimization on non-volatile main memory **2011**,		11

113	Combining Coarse-Grained Software Pipelining with DVS for Scheduling Real-Time Periodic Dependent Tasks on Multi-Core Embedded Systems. *Journal of Signal Processing Systems*, **2009**, 57, 249-262	1.4	11
112	State Asymmetry Driven State Remapping in Phase Change Memory. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2017**, 36, 27-40	2.5	10
111	MGC: Multiple graph-coloring for non-volatile memory based hybrid Scratchpad Memory **2012**,		10
110	Exploiting process variation for retention induced refresh minimization on flash memory **2016**,		10
109	Maximizing IO performance via conflict reduction for flash memory storage systems **2015**,		10
108	EMC: Energy-Aware Morphable Cache Design for Non-Volatile Processors. *IEEE Transactions on Computers*, **2019**, 68, 498-509	2.5	10
107	Migration-Aware Loop Retiming for STT-RAM-Based Hybrid Cache in Embedded Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 329-342	2.5	9
106	Exploit asymmetric error rates of cell states to improve the performance of flash memory storage systems **2014**,		9
105	Minimizing write activities to non-volatile memory via scheduling and recomputation **2010**,		9
104	Register allocation for hybrid register architecture in nonvolatile processors **2014**,		8
103	A Unified Write Buffer Cache Management Scheme for Flash Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2779-2792	2.6	8
102	Register allocation for write activity minimization on non-volatile main memory for embedded systems. *Journal of Systems Architecture*, **2012**, 58, 13-23	5.5	8
101	Cache coherence enabled adaptive refresh for volatile STT-RAM **2013**,		8
100	Power-Aware Variable Partitioning for DSPs With Hybrid PRAM and DRAM Main Memory. *IEEE Transactions on Signal Processing*, **2013**, 61, 3509-3520	4.8	8
99	Sleep-aware variable partitioning for energy-efficient hybrid PRAM and DRAM main memory **2014**,		8
98	Acceleration of Composite Order Bilinear Pairing on Graphics Hardware. *Lecture Notes in Computer Science*, **2012**, 341-348	0.9	8
97	An I/O Scheduling Strategy for Embedded Flash Storage Devices With Mapping Cache. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 756-769	2.5	8
96	Exploiting Chip Idleness for Minimizing Garbage Collection-Induced Chip Access Conflict on SSDs. *ACM Transactions on Design Automation of Electronic Systems*, **2018**, 23, 1-29	1.5	8

95	Online OLED dynamic voltage scaling for video streaming applications on mobile devices **2013**,		7
94	Maximizing Forward Progress with Cache-aware Backup for Self-powered Non-volatile Processors **2017**,		7
93	Training neural-network-based controller on distributed machine learning platform for power electronics systems **2017**,		7
92	Scheduling to Optimize Cache Utilization for Non-Volatile Main Memories. *IEEE Transactions on Computers*, **2014**, 63, 2039-2051	2.5	7
91	Optimizing Data Allocation and Memory Configuration for Non-Volatile Memory Based Hybrid SPM on Embedded CMPs **2012**,		7
90	Instruction Cache Locking for Real-Time Embedded Systems with Multi-tasks **2009**,		7
89	Optimized address assignment with array and loop transformations for minimizing schedule length. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2008**, 55, 379-389	3.9	7
88	Address assignment sensitive variable partitioning and scheduling for DSPS with multiple memory banks. *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, **2008**,	1.6	7
87	A Wear Leveling Aware Memory Allocator for Both Stack and Heap Management in PCM-based Main Memory Systems **2019**,		6
86	An empirical study of F2FS on mobile devices **2017**,		6
85	LADPM: Latency-Aware Dual-Partition Multicast Routing for Mesh-Based Network-on-Chips **2010**,		6
84	Towards energy efficient hybrid on-chip Scratch Pad Memory with non-volatile memory **2011**,		6
83	Sleep-aware mode assignment in wireless embedded systems. *Journal of Parallel and Distributed Computing*, **2011**, 71, 1002-1010	4.4	6
82	1+1>2: variation-aware lifetime enhancement for embedded 3D NAND flash systems **2019**,		5
81	Energy Optimal Task Scheduling with Normally-Off Local Memory and Sleep-Aware Shared Memory with Access Conflict. *IEEE Transactions on Computers*, **2018**, 1-1	2.5	5
80	NVM-Based FPGA Block RAM With Adaptive SLC-MLC Conversion. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2661-2672	2.5	5
79	WCET-Aware Re-Scheduling Register Allocation for Real-Time Embedded Systems With Clustered VLIW Architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 168-180	2.6	5
78	Energy-aware morphable cache management for self-powered non-volatile processors **2017**,		5

77	Maximizing common idle time on multi-core processors with shared memory **2015**,		5
76	Branch Prediction-Directed Dynamic Instruction Cache Locking for Embedded Systems. *Transactions on Embedded Computing Systems*, **2014**, 13, 1-24	1.8	5
75	Optimal task allocation on non-volatile memory based hybrid main memory **2011**,		5
74	Optimizing Scheduling and Intercluster Connection for Application-Specific DSP Processors. *IEEE Transactions on Signal Processing*, **2009**, 57, 4538-4547	4.8	5
73	Compiler directed write-mode selection for high performance low power volatile PCM. *ACM SIGPLAN Notices*, **2013**, 48, 101-110	0.2	5
72	File Fragmentation in Mobile Devices: Measurement, Evaluation, and Treatment. *IEEE Transactions on Mobile Computing*, **2019**, 18, 2062-2076	4.6	5
71	Checkpointing-Aware Loop Tiling for Energy Harvesting Powered Nonvolatile Processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 15-28	2.5	5
70	Boosting the Performance of SSDs via Fully Exploiting the Plane Level Parallelism. *IEEE Transactions on Parallel and Distributed Systems*, **2020**, 31, 2185-2200	3.7	4
69	Race to idle or not: balancing the memory sleep time with DVS for energy minimization. *Journal of Combinatorial Optimization*, **2018**, 35, 860-894	0.9	4
68	Real-Time Data Retrieval With Multiple Availability Intervals in CPS Under Freshness Constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2743-2754	2.5	4
67	Minimizing accumulative memory load cost on multi-core DSPs with multi-level memory. *Journal of Systems Architecture*, **2013**, 59, 389-399	5.5	4
66	DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2981-2994	2.6	4
65	Retention trimming for wear reduction of flash memory storage systems **2014**,		4
64	Write Mode Aware Loop Tiling for High Performance Low Power Volatile PCM **2014**,		4
63	WCET-aware re-scheduling register allocation for real-time embedded systems with clustered VLIW architecture **2012**,		4
62	Timing optimization via nest-loop pipelining considering code size. *Microprocessors and Microsystems*, **2008**, 32, 351-363	2.4	4
61	Energy, latency, and lifetime improvements in MLC NVM with enhanced WOM code **2018**,		3
60	Write Mode Aware Loop Tiling for High Performance Low Power Volatile PCM in Embedded Systems. *IEEE Transactions on Computers*, **2016**, 65, 2313-2324	2.5	3

59	A wear-leveling-aware dynamic stack for PCM memory in embedded systems **2014**,		3
58	Loop fusion and reordering for register file optimization on stream processors. *Journal of Systems and Software*, **2012**, 85, 1673-1681	3.3	3
57	Memory access schedule minimization for embedded systems. *Journal of Systems Architecture*, **2012**, 58, 48-59	5.5	3
56	Migration-aware loop retiming for STT-RAM based hybrid cache for embedded systems **2013**,		3
55	Joint WCET and Update Activity Minimization for Cyber-Physical Systems. *Transactions on Embedded Computing Systems*, **2015**, 14, 1-21	1.8	3
54	Code Motion for Migration Minimization in STT-RAM Based Hybrid Cache **2012**,		3
53	Register allocation for embedded systems to simultaneously reduce energy and temperature on registers. *Transactions on Embedded Computing Systems*, **2013**, 13, 1-26	1.8	3
52	Energy-Efficient Joint Scheduling and Application-Specific Interconnection Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1813-1822	2.6	3
51	Analysis and approximation for bank selection instruction minimization on partitioned memory architecture **2010**,		3
50	Optimal scheduling to minimize non-volatile memory access time with hardware cache **2010**,		3
49	Real-Time Loop Scheduling with Leakage Energy Minimization for Embedded VLIW DSP Processors. *Gifted and Talented International*, **2007**,	1	3
48	Dynamic merging/splitting for better responsiveness in mobile devices **2016**,		3
47	Process Variation Aware Read Performance Improvement for LDPC-Based nand Flash Memory. *IEEE Transactions on Reliability*, **2020**, 69, 310-321	4.6	3
46	Work-in-Progress: Revisiting Wear Leveling Design on Compression Applied 3D NAND Flash Memory **2018**,		3
45	Maximizing Common Idle Time on Multicore Processors With Shared Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2095-2108	2.6	2
44	Improving MLC PCM write throughput by write reconstruction **2015**,		2
43	C3: Cooperative Code Positioning and Cache Locking for WCET Minimization **2015**,		2
42	Access Characteristic Guided Read and Write Regulation on Flash Based Storage Systems. *IEEE Transactions on Computers*, **2018**, 67, 1663-1676	2.5	2

41	Real-Time Data Retrieval in Cyber-Physical Systems with Temporal Validity and Data Availability Constraints. *IEEE Transactions on Knowledge and Data Engineering*, **2019**, 31, 1779-1793	4.2	2
40	Reinforcement Learning based Background Segment Cleaning for Log-structured File System on Mobile Devices **2019**,		2
39	Thread Criticality Assisted Replication and Migration for Chip Multiprocessor Caches. *IEEE Transactions on Computers*, **2017**, 66, 1747-1762	2.5	2
38	Joint Profit and Process Variation Aware High Level Synthesis With Speed Binning. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1640-1650	2.6	2
37	Compiler directed write-mode selection for high performance low power volatile PCM **2013**,		2
36	Energy-aware register file re-partitioning for clustered VLIW architectures **2009**,		2
35	**2011**,		2
34	Minimizing Memory Access Schedule for Memories **2009**,		2
33	Effective Loop Partitioning and Scheduling under Memory and Register Dual Constraints **2008**,		2
32	Applying Multiple Level Cell to Non-volatile FPGAs. *Transactions on Embedded Computing Systems*, **2020**, 19, 1-22	1.8	2
31	Race to idle or not: Balancing the memory sleep time with DVS for energy minimization **2015**,		2
30	Peak-to-average pumping efficiency improvement for charge pump in Phase Change Memories **2016**,		2
29	Shadow Block: Accelerating ORAM Accesses with Data Duplication **2018**,		2
28	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2153-2163	2.6	1
27	Improving read performance via selective Vpass reduction on high density 3D NAND flash memory **2017**,		1
26	A wear-leveling-aware dynamic stack for PCM memory in embedded systems **2014**,		1
25	Analysis and approximation for bank selection instruction minimization on partitioned memory architecture. *Journal of Combinatorial Optimization*, **2012**, 23, 274-291	0.9	1
24	**2013**,		1

23	Thread Progress Aware Coherence Adaption for Hybrid Cache Coherence Protocols. *IEEE Transactions on Parallel and Distributed Systems*, **2014**, 25, 2697-2707	3.7	1
22	Dual partitioning multicasting for high-performance on-chip networks. *Journal of Parallel and Distributed Computing*, **2014**, 74, 1858-1871	4.4	1
21	Poster Abstract: Smart Phone Lift for Improving Energy Efficiency and User Comfort in Green Buildings **2012**,		1
20	Compiler-assisted refresh minimization for volatile STT-RAM cache **2013**,		1
19	Data re-allocation enabled cache locking for embedded systems **2013**,		1
18	Co-optimization of memory access and task scheduling on MPSoC architectures with multi-level memory **2010**,		1
17	Joint variable partitioning and bank selection instruction optimization on embedded systems with multiple memory banks **2010**,		1
16	TEACA: Thread ProgrEss Aware Coherence Adaption for hybrid coherence protocols **2012**,		1
15	Variable Length Pattern Matching for Hardware Network Intrusion Detection System. *Journal of Signal Processing Systems*, **2010**, 59, 85-93	1.4	1
14	A Formal Specification and Verification Framework for Designing and Verifying Reliable and Dependable Software for Computerized Numerical Control (CNC) Systems **2008**,		1
13	Minimizing Leakage Energy with Modulo Scheduling for VLIW DSP Processors. *International Federation for Information Processing*, **2008**, 111-120		1
12	Minimizing cell-to-cell interference by exploiting differential bit impact characteristics of scaled MLC NAND flash memories **2016**,		1
11	Read-Ahead Efficiency on Mobile Devices: Observation, Characterization, and Optimization. *IEEE Transactions on Computers*, **2021**, 70, 99-110	2.5	1
10	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1782-1795	2.5	1
9	Algorithms to Minimize Data Transfer for Code Update on Wireless Sensor Network. *Journal of Signal Processing Systems*, **2013**, 71, 143-157	1.4	
8	Guest Editorial Special Section on Memory Architectures and Organization. *IEEE Embedded Systems Letters*, **2012**, 4, 81-81	1	
7	Joint variable partitioning and bank selection instruction optimization for partitioned memory architectures. *Transactions on Embedded Computing Systems*, **2013**, 12, 1-27	1.8	
6	Migration-aware adaptive MPSoC static schedules with dynamic reconfigurability. *Journal of Parallel and Distributed Computing*, **2011**, 71, 1400-1410	4.4	

List of Publications

5	Analysis and approximation for bank selection instruction minimization on partitioned memory architecture. *ACM SIGPLAN Notices*, **2010**, 45, 1-8	0.2
4	NetKernel: Making Network Stack Part of the Virtualized Infrastructure. *IEEE/ACM Transactions on Networking*, **2021**, 1-15	3.8
3	Single and Multiple Device DSA Problem, Complexities and Online Algorithms. *Lecture Notes in Computer Science*, **2010**, 218-229	0.9
2	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5
1	Online Rare Category Identification and Data Diversification for Edge Computing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5