Kanad Basu

List of Publications by Year
in descending order

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36	585	933447	794594
papers	citations	10	19
		h-index	g-index

36	36	36	311
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Analysis and Mitigation of DRAM Faults in Sparse-DNN Accelerators. IEEE Design and Test, 2023, 40, 90-99.	1.2	0
2	Real-Time Hardware-Based Malware and Micro-Architectural Attack Detection Utilizing CMOS Reservoir Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 349-353.	3.0	1
3	RTL-ConTest: Concolic Testing on RTL for Detecting Security Vulnerabilities. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 466-477.	2.7	7
4	Runtime Malware Detection Using Embedded Trace Buffers. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 35-48.	2.7	2
5	Explainable Machine Learning for Intrusion Detection via Hardware Performance Counters. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4952-4964.	2.7	9
6	Special Session: Effective In-field Testing of Deep Neural Network Hardware Accelerators. , 2022, , .		0
7	Defending Hardware-Based Malware Detectors Against Adversarial Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1727-1739.	2.7	10
8	Satisfiability Attack-Resistant Camouflaged Two-Dimensional Heterostructure Devices. ACS Nano, 2021, 15, 3453-3467.	14.6	24
9	Hardware-assisted Detection of Malware in Automotive-Based Systems. , 2021, , .		1
10	Toward Functional Safety of Systolic Array-Based Deep Learning Hardware Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 485-498.	3.1	33
11	HardCompress: A Novel Hardware-based Low-power Compression Scheme for DNN Accelerators. , 2021, , .		3
12	Special Session: Reliability Analysis for AI/ML Hardware. , 2021, , .		18
13	Can Overclocking Detect Hardware Trojans?. , 2021, , .		2
14	Two Sides of the Same Coin: Boons and Banes of Machine Learning in Hardware Security. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 228-251.	3.6	4
15	Hardware Performance Counters: Ready-Made vs Tailor-Made. Transactions on Embedded Computing Systems, 2021, 20, 1-26.	2.9	1
16	Hardware-assisted detection of firmware attacks in inverter-based cyberphysical microgrids. International Journal of Electrical Power and Energy Systems, 2021, 132, 107150.	5.5	28
17	WiND: An Efficient Post-Silicon Debug Strategy for Network on Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2372-2385.	2.7	5
18	In situ ellipsometry aided rapid ALD process development and parameter space visualization of cerium oxide nanofilms. Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films, 2021, 39, .	2.1	3

#	Article	IF	Citations
19	Time Series-Based Malware Detection Using Hardware Performance Counters. , 2021, , .		2
20	Post-Silicon Gate-Level Error Localization With Effective and Combined Trace Signal Selection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 248-261.	2.7	12
21	Toward Increasing the Difficulty of Reverse Engineering of RSFQ Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-13.	1.7	14
22	A Theoretical Study of Hardware Performance Counters-Based Malware Detection. IEEE Transactions on Information Forensics and Security, 2020, 15, 512-525.	6.9	40
23	COPPTCHA: COPPA Tracking by Checking Hardware-Level Activity. IEEE Transactions on Information Forensics and Security, 2020, 15, 3213-3226.	6.9	8
24	Hardware Trojan Detection Using Controlled Circuit Aging. IEEE Access, 2020, 8, 77415-77434.	4.2	19
25	Benefits and Challenges of Utilizing Hardware Performance Counters for COPPA Violation Detection. , 2020, , .		1
26	ND-HMDs: Non-Differentiable Hardware Malware Detectors against Evasive Transient Execution Attacks. , 2020, , .		6
27	Hardware Trojans Inspired IP Watermarks. IEEE Design and Test, 2019, 36, 72-79.	1.2	11
28	PREEMPT. , 2019, , .		16
29	Fault-Tolerant Systolic Array Based Accelerators for Deep Neural Network Execution. IEEE Design and Test, 2019, 36, 44-53.	1.2	54
30	Can Monitoring System State + Counting Custom Instruction Sequences Aid Malware Detection?. , 2019, , .		2
31	Analyzing and mitigating the impact of permanent faults on a systolic array based neural network accelerator. , 2018, , .		101
32	RATS: Restoration-Aware Trace Signal Selection for Post-Silicon Validation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 605-613.	3.1	64
33	Constrained signal selection for post-silicon validation. , 2012, , .		3
34	Efficient Trace Signal Selection for Post Silicon Validation and Debug. , 2011, , .		38
35	Efficient combination of trace and scan signals for post silicon validation and debug. , 2011, , .		24
36	Efficient trace data compression using statically selected dictionary. , 2011, , .		19