Kiyoung Choi

List of Publications by Citations

78 papers	862 citations	18 h-index	25 g-index
115 ext. papers	1,111 ext. citations	2.2 avg, IF	4.27 L-index

#	Paper	IF	Citations
78	Power conscious fixed priority scheduling for hard real-time systems		60
77	DASCA: Dead Write Prediction Assisted STT-RAM Cache Architecture **2014**,		57
76	Partial bus-invert coding for power optimization of application-specific systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2001**, 9, 377-383	2.6	47
75	Deep neural networks with weighted spikes. *Neurocomputing*, **2018**, 311, 373-386	5.4	40
74	Mapping Multi-Domain Applications Onto Coarse-Grained Reconfigurable Architectures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 637-650	2.5	36
73	Power optimization of real-time embedded systems on variable speed processors		34
72	An energy-efficient random number generator for stochastic circuits **2016**,		32
71	Prediction Hybrid Cache: An Energy-Efficient STT-RAM Cache Architecture. *IEEE Transactions on Computers*, **2016**, 65, 940-951	2.5	28
70	FloRA: Coarse-grained reconfigurable architecture with floating-point operation capability **2009**,		28
69	Power-conscious configuration cache structure and code mapping for coarse-grained reconfigurable architecture **2006**,		26
68	Exploiting New Interconnect Technologies in On-Chip Communication. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 124-136	5.2	23
67	Approximate de-randomizer for stochastic circuits **2015**,		22
66	Write intensity prediction for energy-efficient non-volatile caches **2013**,		21
65	ExtraV. *Proceedings of the VLDB Endowment*, **2017**, 10, 1706-1717	3.1	20
64	Accurate and Efficient Stochastic Computing Hardware for Convolutional Neural Networks **2017**,		19
63	Low Power Reconfiguration Technique for Coarse-Grained Reconfigurable Architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2009**, 17, 593-603	2.6	19
62	SoCDAL. *ACM Transactions on Design Automation of Electronic Systems*, **2008**, 13, 1-38	1.5	19

61	Performance-driven high-level synthesis with bit-level chaining and clock selection. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2001**, 20, 199-212	2.5	19
60	Design Space Exploration for Efficient Resource Utilization in Coarse-Grained Reconfigurable Architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1471-1482	2.6	18
59	Scalable stochastic-computing accelerator for convolutional neural networks **2017**,		15
58	Communication Architecture Synthesis of Cascaded Bus Matrix **2007**,		14
57	Design space exploration of FPGA accelerators for convolutional neural networks **2017**,		13
56	Narrow bus encoding for low-power DSP systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2001**, 9, 656-660	2.6	13
55	Partial bus-invert coding for power optimization of system level bus		13
54	Dynamic Power Management of Off-Chip Links for Hybrid Memory Cubes **2014**,		12
53	Mapping and Scheduling of Tasks and Communications on Many-Core SoC Under Local Memory Constraint. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1748-1761	2.5	12
52	Scheduler implementation in MP SoC design **2005**,		12
51	Lower-bits cache for low power STT-RAM caches **2012**,		11
50	Delay Monitoring System With Multiple Generic Monitors for Wide Voltage Range Operation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 37-49	2.6	8
49	Thermal-aware fault-tolerant system design with coarse-grained reconfigurable array architecture **2010**,		8
48	Automatic mapping of application to coarse-grained reconfigurable architecture based on high-level synthesis techniques **2008**,		8
47	Low-Power Hybrid Memory Cubes With Link Power Management and Two-Level Prefetching. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 453-464	2.6	7
46	Adaptively weighted round-robin arbitration for equality of service in a many-core network-on-chip. *IET Computers and Digital Techniques*, **2016**, 10, 37-44	0.9	7
45	An FPGA implementation of high-throughput key-value store using Bloom filter **2014**,		7
44	A deadlock-free routing algorithm requiring no virtual channel on 3D-NoCs with partial vertical connections **2013**,		7

43	Exploration of trade-offs in the design of volatile STTRAM cache. *Journal of Systems Architecture*, **2016**, 71, 23-31	5.5	6
42	Software-Level Approaches for Tolerating Transient Faults in a Coarse-GrainedReconfigurable Architecture. *IEEE Transactions on Dependable and Secure Computing*, **2014**, 11, 392-398	3.9	6
41	Isomorphism-Aware Identification of Custom Instructions With I/O Serialization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 34-46	2.5	6
40	Scheduling with accurate communication delay model and scheduler implementation for multiprocessor system-on-chip. *Design Automation for Embedded Systems*, **2007**, 11, 167-191	0.6	6
39	Energy-efficient partitioning of hybrid caches in multi-core architecture **2014**,		5
38	Position-based weighted round-robin arbitration for equality of service in many-core network-on-chips **2012**,		5
37	Enforcing schedulability of multi-task systems by hardware-software codesign		5
36	Performance improvement of multi-processor systems cosimulation based on SW analysis		5
35	ComPEND **2018**,		5
34	Buffered compares: Excavating the hidden parallelism inside DRAM architectures with lightweight logic **2016**,		5
33	Aging Compensation With Dynamic Computation Approximation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 1319-1332	3.9	4
32	An Efficient and Accurate Stochastic Number Generator Using Even-Distribution Coding. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 3056-3066	2.5	4
31	Aging Gracefully with Approximation **2019**,		4
30	An approach to code compression for CGRA **2011**,		4
29	Excavating the Hidden Parallelism Inside DRAM Architectures With Buffered Compares. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1793-1806	2.6	3
28	LASIC: Loop-Aware Sleepy Instruction Caches Based on STT-RAM Technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1197-1201	2.6	3
27	Active Memory Processor for Network-on-Chip-Based Architecture. *IEEE Transactions on Computers*, **2012**, 61, 622-635	2.5	3
26	FPGA implementation of convolutional neural network based on stochastic computing **2017**,		3

25	Automatic mapping of control-intensive kernels onto coarse-grained reconfigurable array architecture with speculative execution **2010**,		3
24	An adaptive routing algorithm for 3D mesh NoC with limited vertical bandwidth **2012**,		3
23	Loop pipelining in hardware-software partitioning		3
22	Optimizing Timed Cosimulation by Hybrid Synchronization. *Design Automation for Embedded Systems*, **2000**, 5, 129-152	0.6	3
21	Optimizing geographically distributed timed cosimulation by hierarchically grouped messages		3
20	A polynomial-time custom instruction identification algorithm based on dynamic programming **2011**,		2
19	High-level synthesis with distributed controller for fast timing closure **2011**,		2
18	Communication architecture design for reconfigurable multimedia SoC platform. *Design Automation for Embedded Systems*, **2010**, 14, 1-20	0.6	2
17	An Integrated Cosimulation Environment for Heterogeneous Systems Prototyping. *Design Automation for Embedded Systems*, **1998**, 3, 163-186	0.6	2
16	Fast cycle-approximate MPSoC simulation based on synchronization time-point prediction. *Design Automation for Embedded Systems*, **2007**, 11, 223-247	0.6	2
15	Automatic Bus Matrix Synthesis based on Hardware Interface Selection for Fast Communication Design Space Exploration **2007**,		2
14	Interleaving partial bus-invert coding for low power reconfiguration of FPGAs		2
13	Hybrid spiking-stochastic Deep Neural Network **2017**,		1
12	Optimal mapping of program overlays onto many-core platforms with limited memory capacity. *Design Automation for Embedded Systems*, **2017**, 21, 173-194	0.6	1
11	Leveraging parallelism in the presence of control flow on CGRAs **2014**,		1
10	A formal approach toward developing an equivalent circuit for high-speed coupled interconnects with intermediate ground insertion **2010**,		1
9	A host-accelerator communication architecture design for efficient binary acceleration **2011**,		1
8	Resource-shared custom instruction generation under performance/area constraints **2012**,		1

7	ODALRISC: A small, low power, and configurable 32-bit RISC processor **2008**,		1
6	Hardware-software cosynthesis for run-time incrementally reconfigurable FPGAs		1
5	An Efficient Simulation Environment and Simulation Techniques for Bluetooth Device Design. *Design Automation for Embedded Systems*, **2003**, 8, 119-138	0.6	0
4	Guest Editorial for Special Issue on Emerging Memory Technologies Modeling, Design, and Applications for Multi-Scale Computing. *IEEE Transactions on Multi-Scale Computing Systems*, **2015**, 1, 125-126		
3	Guest Editorial New Interconnect Technologies in On-Chip Communication. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 121-123	5.2	
2	ESL Design Methodology. *Journal of Electrical and Computer Engineering*, **2012**, 2012, 1-2	1.9	
1	ComPreEND: Computation Pruning through Predictive Early Negative Detection for ReLU in a Deep Neural Network Accelerator. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	